G80F975A

Single-phase Energy Metering IC integrated LCD driver and enhanced 8051 Microcontroller

Rev1.00 2019.12

Selection Guide

ORDER TYPE	FLASH	RAM	data flash	I/O MAX	TIMER	INT	ADC	EUART	LCD	Other	TEMPERATURE RANGE	PACKAGE
G80F975A	128K	8232	4K	47	3*16	4	1*14	3	4*28 6*26 8*24	JTAG/RTC/EMU /LPD/LVR/WDT	-40℃～+85℃	LQFP64

Catalogue

1.Features

8051 compatible Pipe-lined instruction based on the single-chip 8-bit micro-controller
Flash ROM：128K Bytes
EEPROM：4K Bytes (shared with Flash room)
RAM：internal 256 Bytes，and external 7936 Bytes
LCD RAM：40 Bytes
Waveform sampling: 1536 Bytes (Waveform sampling)
Operation voltage：2.3V – 5.5V
Oscillator (Code option)：
- fOSC：32.768kHz
- Build in PLL：PLL=131kHz/4 RC
- Build in PLL：PLL=8M C(Touch_Key and Temperature sensor Clock Source)
- Built-in SCM，32.768 suspension was replaced by 32.75kHz RC.
80 CMOS general purpose I/O ports
Built-in pull-up resistor for I/O
Three 16-bit timer / counters: T0，T1&T2
Powerful interrupt sources：
- Timer0, Timer1, Timer2
- External interrupt 4
- EUART0，EUART1，EUART3
- RTC
- ADC/TPS，EMU，LPD1

1 channels 14-bit Analog to Digital Converter（ADC）
Energy Metering
Active/ reactive/ apparent Energy Metering and voltage/ current rms metering
Accuracy of 0.1% for active energy over a dynamic range of 3000:1
Accuracy of 0.5% for reactive energy over a dynamic range of 1500:1
Less than 0.5% error for voltage/ current rms
Current Detection
DC Metering
Low power consumption measurement mode, low to 800uA(3 road ADC, drop line mode)
Built-in waveform sampling store Functio.n
3 bit EUART, Build in IR
Build in low power RTC
Build in Temperature sensor+/-1℃ (-40~+85℃)
Automatic switching of battery power
LCD driver：
- 4 COM X 28EG（1/4 duty 1/3 bias）
- 6 COM X 26EG（1/6 duty 1/3 bias）
- 8 COM X 24EG（1/8 duty 1/4 bias）
- 8 Level contrast software adjustment.

Built-in low power detection（LPD）
Built-in low voltage reset (LVR) function (enabled by code option)
LVR voltage：2.4V
Built-in Watch Dog Timer（WDT）
Warm-up timer for power-on reset
CPU Machine cycle: 1 oscillator clock
Support Low power operation modes：
- IDLE Mode
- Power-Down Mode (Power 3.5uA)

-Package:LQFP64

2.General Description

The G80F975A is a low-cost,high-performance single-phase energy metering SOC chip, and integrated single-phase energy metering, LCD driver, Calendar clock and enhanced 8051 microcontroller.

G80F975A embedded energy metering module, to measure active, reactive and apparent energy, as well as voltage/ current rms. And then to monitor the voltage sag of the power line and zero-crossing features。

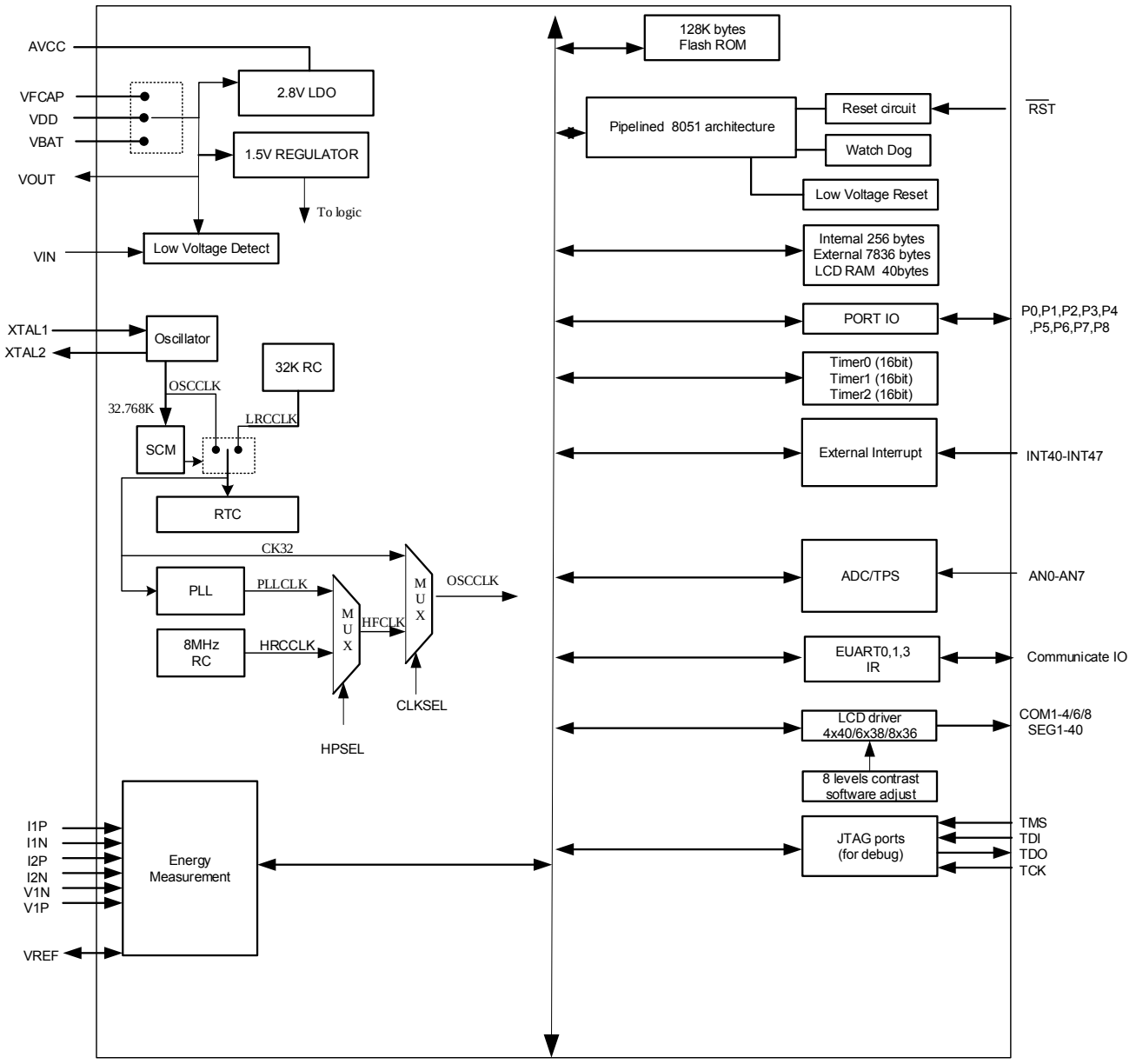
The G80F975A is a fast 8051 compatible micro-controller with a redesigned CPU of no wasted clock and memory cycles. Typically, it will be faster and exhibit better performance than the traditional 8051 at the same oscillator frequency.

The G80F975A retains most features of the standard 8051. These features include internal 256 bytes RAM, two 16-bit timers / counters(Timer0/Timer1), 3 UART ,and external interrupt INT4. In addition, the G80F975A provides external 7936 bytes RAM (not include LCD RAM), 16-bit timer/counter (Timer2) compatible with 8052. It contains a 128K Bytes Flash memory block for program and data.

Some standard serial communication modes such as EUART、IR are supported in G80F975A. Also the LCD driver, ADC and RTC are incorporated in G80F975A.

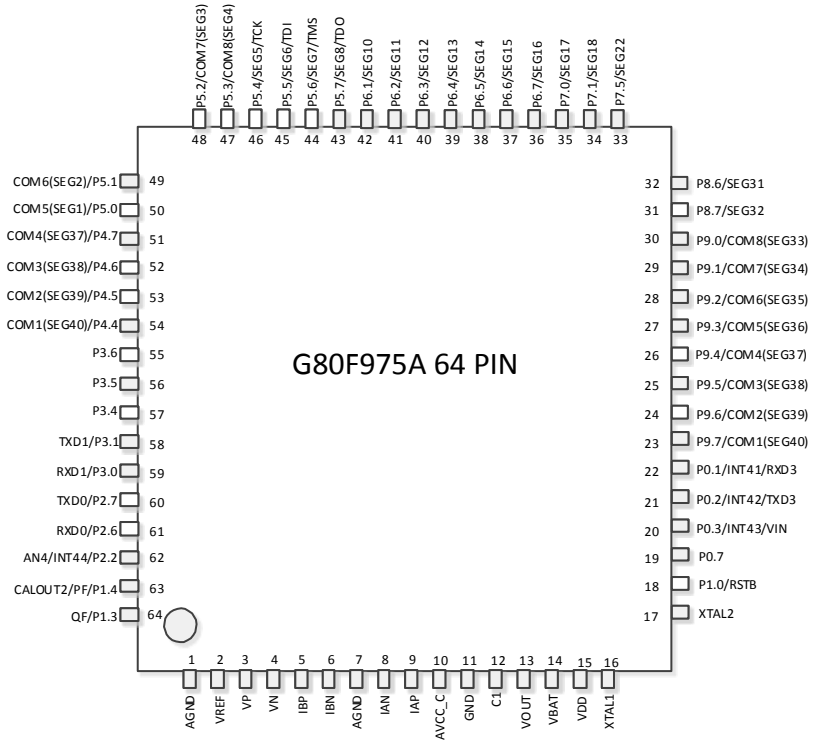
For high reliability and low cost issues, the G80F975A builds in PLL clock, Watchdog Timer, Low Voltage Reset function, and oscillator fail detection. G80F975A also supports two power supply modes and two power saving modes to reduce power consumption.

3.Block Diagram



Note: the actual chip VFCAP is not extracted. The pin inside the chip is connected to VBAT.

4.Pin Configuration



LQFP64 Pin Configuration Diagram

Note: The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram). This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Only until the higher priority function is disabled by software, can the corresponding pin be released for the lower priority function use.

Table 4.1 Pin Functions

64PIN NO.	Pin Name	Default function	64PIN NO.	Pin Name	Default function
1	AGND	------	33	SEG22/P7.5	P7.5
2	VREF	------	34	SEG18/P7.1	P7.1
3	VP	------	35	SEG17/P7.0	P7.0
4	VN	------	36	SEG16/P6.7	P6.7
5	IBP	------	37	SEG15/P6.6	P6.6
6	IBN	------	38	SEG14/P6.5	P6.5
7	AGND	------	39	SEG13/P6.4	P6.4
8	IAN	------	40	SEG12/P6.3	P6.3
9	IAP	------	41	SEG11/P6.2	P6.2
10	AVCC_C	------	42	SEG10/P6.1	P6.1
11	GND	------	43	TDO/SEG8 /P5.7	P5.7
12	C1	------	44	TMS/SEG7 /P5.6	P5.6
13	VOUT	------	45	TDI/SEG6 /P5.5	P5.5
14	VBAT	------	46	TCK/SEG5 /P5.4	P5.4
15	VDD	------	47	COM8/SEG4 /P5.3	P5.3
16	XTAL1	------	48	COM7/SEG3 /P5.2	P5.2
17	XTAL2	------	49	COM6/SEG2 /P5.1	P5.1
18	P1.0/RSTB	P1.0	50	COM5/SEG1 /P5.0	P5.0
19	P0.7	P0.7	51	COM4(SEG37) /P4.7	P4.7
20	VIN/INT43/P0.3	P0.3	52	COM3(SEG38)/P4.6	P4.6
21	TXD3/INT42/P0.2	P0.2	53	COM2(SEG39) /P4.5	P4.5
22	RXD3/INT41/P0.1	P0.1	54	COM1(SEG40)/P4.4	P4.4
23	SEG40(COM1)/P9.7	P9.7	55	P3.6	P3.6
24	SEG39(COM2)/P9.6	P9.6	56	P3.5	P3.5
25	SEG38(COM3)/P9.5	P9.5	57	P3.4	P3.4
26	SEG37(COM4)/P9.4	P9.4	58	TXD1/P3.1	P3.1
27	COM5/SEG36/P9.3	P9.3	59	RXD1/P3.0	P3.0
28	COM6/SEG35/P9.2	P9.2	60	TXD0/P2.7	P2.7
29	COM7/SEG34/P9.1	P9.1	61	RXD0/P2.6	P2.6
30	COM8/SEG33/P9.0	P9.0	62	AN4/INT44/P2.2	P2.2
31	SEG32/P8.7	P8.7	63	CALOUT2/PF/P1.4	P1.4
32	SEG31/P8.6	P8.6	64	QF/P1.3	P1.3

5.Pin Description

Pin Name	Type	Description
PORT		
P0.0 - P0.3, P0.7	I/O	8-bit bi-directional I/O port
P0.0 - P0.3, P0.7	I/O	8-bit bi-directional I/O port
P2.2, P2.6, P2.7	I/O	8-bit bi-directional I/O port
P3.0, P3.1, P3.4-P3.6	I/O	8-bit bi-directional I/O port
P4.4 - P4.7	I/O	8-bit bi-directional I/O port
P5.0 – P5.7	I/O	8-bit bi-directional I/O port
P6.1 – P6.7	I/O	8-bit bi-directional I/O port
P7.0 , P7.1, P7.5	I/O	8-bit bi-directional I/O port
P8.6, P8.7	I/O	8-bit bi-directional I/O port
P9.0 – P9.7	I/O	8-bit bi-directional I/O port
EUART		
RXD0	I/O	EUART0 data input/ output
TXD0	O	EUART0 data output.
RXD1	I/O	EUART1 data input/ output
TXD1	O	EUART1 data output.
RXD3	I/O	EUART3 data input/ output
TXD3	O	EUART3 data output.
LCD controller		
COM1 - COM8	O	Common signal output for LCD display
SEG1 – SEG40	O	Segment signal output for LCD display

Pin No	Type	Description
RTC		
CALOUT2	O	Compensation clock output2
Interrupt & Reset & Clock & Power		
INT40 – INT47	I	External interrupt
$\overline{\text{RST}}$	I	A low on this pin for 10us longer will reset the device. An internal diffused resistor to VDD permits a power-on reset using only an external capacitor to GND.
XTAL1	I	Oscillator input
XTAL2	O	Oscillator output
GND	P	Digital ground
AGND	P	Analog ground，PCB connect GND
VDD	P	Power
VBAT	P	Battery supply
C1	P	Digital power supply circuit,the external need to connect the 4.7uF capacitor to ground,the typical voltage 1.55V
VOUT	P	Power output pin（output VDD or VBAT by using a switch）, digital circuit supply.
AVCC_C	P	Energy Metering Analog Power with built-in 2.8V LDO output. It requires an 1uF external ceramic capacitor to GND.
ADC		
AN4	I	ADC input chanels
EMU		
IAP,IAN,IBP, IBN;VP,VN	I	Energy metering input
VREF	I/O	Reference voltage input/output requires a translation of 104 capacitors and 105 capacitors to determine whether or not the input and output pins are input.
PF，QF	O	Active/ reactive power pulse output
Programmer		
TDO（SEG8）	O	Debug interface: Test data out
TMS（SEG7）	I	Debug interface: Test mode select
TDI（SEG6）	I	Debug interface: Test data in
TCK（SEG5）	I	Debug interface: Test clock in
Note: When P5.4-5.7 used as debug interface, other functions of P5.4-5.7 are blocked.		
External Voltage detection Pin		
VIN	I	External voltage detection input

6.SFR Mapping

The G80F975A provides 256 bytes of internal RAM to contain general-purpose data memory and Special Function Register (SFR). The SFR of the G80F975A fall into the following categories:

CPU core registers：	ACC，B，PSW，SP，DPL，DPH
Enhanced C51 core registers：	AUXC，DPL1，DPH1，INSCON
Power and clock control registers：	PCON，SUSLO，CLKCON，PWRCON1，PWRCON2，LDOCON，LDOLO，OSCLO
LPD registers：	LPDCON1，LPDCON2
Flash registers：	PBANK，PBANKLO ，IB_OFFSET，XPAGE，IB_DATA，IB_CON1，IB_CON2，IB_CON3，IB_CON4，IB_CON5
Data Memory registe：	XPAGE
Watch-dog registers：	RSTSTAT
Interrupt system registers：	IEN0，IEN1，IPH0，IPL0，IPH1，IPL1，EXF0，IENX，EXCON1，EXCON2
I/O port registers：	P0，P1，P2，P3，P4，P5，P6，P7，P8，P9，P0CR，P1CR，P2CR，P3CR，P4CR，P5CR，P6CR，P7CR，P8CR，P9CR P0PCR，P1PCR，P2PCR，P3PCR，P4PCR，P5PCR，P6PCR，P7PCR，P8PCR，P9PCR P0OS，P2OS，P3OS，P0DRVH，P1DRVL，P2DRVH，P0PHM，P2PHM，P0INM，P2INM
Timer registers：	TCON1，TCON，TMOD，TL0，TH0，TL1，TH1，T2CON，T2MOD， TL2，TH2，RCAP2L，RCAP2H
EUART0 registers：	PCON，SCON，SBUF，SADDR，SADEN，SBRTH，SBRTL，SFINE
EUART1 registers：	SCON1，SBUF1，SADDR1，SADEN1，SBRT1H，SBRT1L
EUART3 registers：	SCON3，SBUF3，SADDR3，SADEN3，SBRT3H，SBRT3L
IR registers：	IRCON1，IRCON2，IRDAT
ADC registers：	ADCON，ADT，ADCH，ADDL，ADDH
LCD registers：	LCDCON1，LCDCON2，P4SS，P5SS, P6SS，P7SS, P8SS，P9SS
PLL registers：	CLKCON
RTC registers：	SBSC，SEC，MIN，HR，DAY，MTH，YR，DOW，RTCDATH，RTCDATL，RTCALM，A0SEC，A0MIN，A0HR，A0DAY，A0DOW，A1SEC，A1MIN，A1HR，RTCCON，RTCWR，RTCPSW，RTCIE，RTCIF，RTCTMR
EMU registers：	EADR，EDTAH，EDTAM，EDTAL，EMUSR，EMUIE，EMUIF

Table 6.1 C51 Core SFRs

Mnem	Addr	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	C Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer1 Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer1 High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 2 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 2 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	----00-0	-	-	-	-	DIV	MUL	-	DPS

Table 6.2 Data MPAGE SFR

Mnem	Addr	Name	POR/WDT/LVR /PINReset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	F7H	Memory Page	00000000	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0

Table 6.3 Power and clock control SFRs

Mnem	Addr	Name	POR/WDT/LVR /PINReset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	00000000	SMOD	SSTAT	SSTAT1	SSTAT2	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
PASLO	E7H	Power select Control	00000000	PASLO.7	PASLO.6	PASLO.5	PASLO.4	PASLO.3	PASLO.2	PASLO.1	PASLO.0
CLKCON	B2H	System Clock Control register	11100000	32K_SPD	CLKS1	CLKS0	SCMF	HFON	CLKSEL	PLLSEL	HFSEL
PWRCON	B3H	Power control register1	-----000	-	-	-	-	-	VOUTS1	VOUTS0	AUTOS
PWRCON	B4H	Power control register1	0000----	LDO28O	LCDLDO1	LCDLDO0	VDDDISC	-	-	-	-
LDOCON	B5H	LDO Control Registers	****-***	LPEN3	LPEN2	LPEN1	LPEN0	-	LDOVOL2	LDOVOL1	LDOVOL0
OSCLO	FEH	System clock lock Registers	00000000	OSCLO.7	OSCLO.6	OSCLO.5	OSCLO.4	OSCLO.3	OSCLO.2	OSCLO.1	OSCLO.0

Table 6.4 LPD control SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON 1	C6H	Low voltage detection control.Registers1	1***000-	LPD1EN	FVIN	LPD1IF	FVDD	LPD1SF	VINITM1	VINITM0	-
LPDCON 2	C7H	Low voltage detection control.Registers2	0*1*0000	LPD2EN	LPD2F	LPD3EN	LPD3F	LPDS3	LPDS2	LPDS1	LPDS0

*note : The initial values vary according to the state of the power supply.

Table 6.5 Flash control SFRs

Mnem	Addr	Name	POR/WDT/LVR /PINReset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	EEH	Low byte offset of flash memory for programming	00000000	IB_OFFSET.7	IB_OFFSET.6	IB_OFFSET.5	IB_OFFSET.4	IB_OFFSET.3	IB_OFFSET.2	IB_OFFSET.1	IB_OFFSET.0
IB_DATA	EFH	Data Register for programming flash memory	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1	F2H	Flash Memory Control Register 1	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2	F3H	Flash Memory Control Register 2	----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3	F4H	Flash Memory Control Register 3	----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4	F5H	Flash Memory Control Register 4	----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5	F6H	Flash Memory Control Register 5	----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
PBANK	B6H	BANK Switch Registers	--01--01	-	-	COBANK.1	COBANK.0	-	-	IFBANK.1	IFBANK.0
PBANKLO	B7H	BANK Switch lock Registers	00000000	PBANKLO.	PBANKLO.	PBANKLO.	PBANKLO.	PBANKLO.	PBANKLO.	PBANKLO.	PBANKLO.
FLASHCO	A7H	FLASH Control Registers	-------0	-	-	-	-	-	-	-	FAC

Table 6.6 WDT SFR

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H	Watchdog Timer Control	*-***000	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

*note : RSTSTAT value will changed in deferent reset condition

Table 6.7 Interrupt SFRs

Mnem	Addr	Name	POR/WDT /LVR/PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H	Interrupt Enable Control 0	00000000	EA	EADTP	ET2	ES0	ET1	-	ET0	EX4
IEN1	A9H	Interrupt Enable Control 1	00000000	ES3	-	ELPD	-	-	ES1	ERTC	EEMU
IENX	AAH	External interrupt channel allows Registers	00000000	EXS47	-	-	EXS44	EXS43	EXS42	EXS41	-
EXF0	ABH	External interrupt 4 flag Registers	0000000-	IF4.7	-	-	IF4.4	IF4.3	IF4.2	IF4.1	-
IPL0	B8H	Interrupt Priority Control Low 0	-0000000	-	PADCL	PT2L	PS0L	PT1L	-	PT0L	PX4L
IPH0	B9H	Interrupt Priority Control High 0	-0000000		PADCH	PT2H	PS0H	PT1H	-	PT0H	PX4H
IPL1	BAH	Interrupt Priority Control Low 1	00000000	PS3L	-	PLPDL	PS2L	-	PS1L	PRTCL	PEMUL
IPH1	BBH	Interrupt Priority Control High 1	00000000	PS3H	-	PLPDH	PS2H	-	PS1H	PRTCH	PEMUH
EXCON1	ABH	External interrupt 4control Registers1	00000000	-	-	IT4.5	IT4.4	IT4.3	IT4.2	IT4.1	IT4.0
EXCON2	ACH	External interrupt 4control Registers2	0000----	I1PS1	I1PS0	IP.1	IP.0	-	-	-	-

Table 6.8 Port SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	80H	8-bit Port 0	0---000-	P0.7	-	-	-	P0.3	P0.2	P0.1	-
P1	90H	8-bit Port 1	---00-0	-	-	-	P1.4	P1.3	-	-	P1.0
P2	A0H	8-bit Port 2	00---0--	P2.7	P2.6	-	-	-	P2.2	-	-
P3	B0H	8-bit Port 3	-000----	-	P3.6	P3.5	P3.4	-	-	-	-
P4	C0H	8-bit Port 4	0000----	P4.7	P4.6	P4.5	P4.4	-	-	-	-
P5	E9H	8-bit Port 5	00000000	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
P6	EAH	8-bit Port 6	0000000-	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	-
P7	EBH	8-bit Port 7	--0---00	-	-	P7.5	-	-	-	P7.1	P7.0
P8	ECH	8-bit Port 8	00------	P8.7	P8.6	-	-	-	-	-	-
P9	EDH	8-bit Port 9	00000000	P9.7	P9.6	P9.5	P9.4	P9.3	P9.2	P9.1	P9.0
P0CR	FFE0H	Port0 input/output direction control	0---000-	P0CR.7	-	-	-	P0CR.3	P0CR.2	P0CR.1	-
P1CR	FFE1H	Port1 input/output direction control	---00-0	-	-	-	P1CR.4	P1CR.3	-	-	P1CR.0

P2CR	FFE2H	Port2 input/output direction control	00---0--	P2CR.7	P2CR.6	-	-	-	P2CR.2	-	-
P3CR	FFE3H	Port3 input/output direction control	-000----	-	P3CR.6	P3CR.5	P3CR.4	-	-	-	-
P4CR	FFE4H	Port4input/output direction control	0000----	P4CR.7	P4CR.6	P4CR.5	P4CR.4	-	-	-	-
P5CR	FFE5H	Port5input/output direction control	00000000	P5CR.7	P5CR.6	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P6CR	FFE6H	Port6 input/output direction control	0000000-	P6CR.7	P6CR.6	P6CR.5	P6CR.4	P6CR.3	P6CR.2	P6CR.1	-
P7CR	FFE7H	Port7 input/output direction control	--0---00	-	-	P7CR.5	-	-	-	P7CR.1	P7CR.0
P8CR	FFE8H	Port8 input/output direction control	00------	P8CR.7	P8CR.6	-	-	-	-	-	-
P9CR	FFE9H	Port9 input/output direction control	00000000	P9CR.7	P9CR.6	P9CR.5	P9CR.4	P9CR.3	P9CR.2	P9CR.1	P9CR.0
P0PCR	FFF0H	Internal pull-high enable for Port0	0---000-	P0PCR.7	-	-	-	P0PCR.3	P0PCR.2	P0PCR.1	-
P1PCR	FFF1H	Internal pull-high enable for Port1	---00-0	-	-	-	P1PCR.4	P1PCR.3	-	-	P1PCR.0
P2PCR	FFF2H	Internal pull-high enable for Port2	00---0--	P2PCR.7	P2PCR.6	-	-	-	P2PCR.2	-	-
P3PCR	FFF3H	Internal pull-high enable for Port3	-000----	-	P3PCR.6	P3PCR.5	P3PCR.4	-	-	-	-
P4PCR	FFF4H	Internal pull-high enable for Port4	0000----	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	-	-	-	-
P5PCR	FFF5H	Internal pull-high enable for Port5	00000000	P5PCR.7	P5PCR.6	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
P6PCR	FFF6H	Internal pull-high enable for Port6	0000000-	P6PCR.7	P6PCR.6	P6PCR.5	P6PCR.4	P6PCR.3	P6PCR.2	P6PCR.1	-
P7PCR	FFF7H	Internal pull-high enable for Port7	--0---00	-	-	P7PCR.5	-	-	-	P7PCR.1	P7PCR.0
P8PCR	FFF8H	Internal pull-high enable for Port8	00------	P8PCR.7	P8PCR.6	-	-	-	-	-	-
P9PCR	FFF9H	Internal pull-high enable for Port9	00000000	P9PCR.7	P9PCR.6	P9PCR.5	P9PCR.4	P9PCR.3	P9PCR.2	P9PCR.1	P9PCR.0
P0OS	FF88H	P0port output mode selectionRegisters	0---000-	P0OS.7	-	-	-	P0OS.3	P0OS.2	P0OS.1	-
P2OS	FF89H	P2port output mode selectionRegisters	00---0--	P2OS.7	P2OS.6	-	-	-	P2OS.2	-	-
P3OS	FF8AH	P3port output mode selectionRegisters	-000--00	-	P3OS.6	P3OS.5	P3OS.4	-	-	P3OS.1	P3OS.0
P0DRVH	FF8BH	P0port output capability selectionRegisters	0---000-	P0DH.7	-	-	-	P0DH.3	P0DH.2	P0DH.1	-

P2DRVH	FF8DH	P2port output capability selectionRegisters	---00--0	-	-	-	P1DL.4	P1DL.3	-	-	P1DL.0
P1DRVL	FF8CH	P1port output capability selectionRegisters	00---0--	P2DH.7	P2DH.6	-	-	-	P2DH.2	-	-
P0PHM	FF8EH	P0 select the upper pull mode Registers	0---000-	P0PH.7	-	-	-	P0PH.3	P0PH.2	P0PH.1	-
P2PHM	FF8FH	P2 select the upper pull mode Registers	00---0--	P2PH.7	P2PH.6	-	-	-	P2PH.2	-	-
P0INM	FFFAH	P0 Input mode selection registers	0---000-	P0INM.7	-	-	-	P0INM.3	P0INM.2	P0INM.1	-
P2INM	FFFBH	P2 Input mode selection registers	00---0--	P2INM.7	P2INM.6	-	-	-	P2INM.2	-	-

Table 6.9 Timer SFRs

Mnem	Addr	Name	POR/WDT/LVR /PINReset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	88H	Timer/Counter 0 ,1Control	0000----	TF1	TR1	TF0	TR0			-	-
TMOD	89H	Timer/Counter 0 ,1Mode	00000000	GATE1	C/$\overline{T1}$	M11	M10	GATE0	C/$\overline{T0}$	M01	M00
TL0	8AH	Timer/Counter 0 Low Byte	00000000	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
TH0	8CH	Timer/Counter 0 High Byte	00000000	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
TL1	8BH	Timer/Counter1 Low Byte	00000000	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.1
TH1	8DH	Timer/Counter 1 High Byte	00000000	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.1
T2CON	C8H	Timer/Counter 2 Control	00--0000	TF2	EXF2	-	-	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9H	Timer/Counter 2 Mode	0------0	TCLKP2	-	-	-	-	-	-	DCEN
RCAP2L	CAH	Timer/Counter 2 Reload/Caprure Low Byte	00000000	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	CBH	Timer/Counter 2 Reload/Caprure High Byte	00000000	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH	Timer/Counter 2 Low Byte	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH	Timer/Counter 2 High Byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
TCON1	8FH	Timer/Counter 0 Control	-00-0000	-	TCLKS1	TCLKS0	-	TCLKP1	TCLKP0	TC1	TC0

Table 6.10 EUART0 SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power & serial Control	00000000	SMOD	SSTAT	SSTAT1	SSTAT2	GF1	GF0	PD	IDL
SCON	98H	Serial Control	00000000	SM0/FE	SM1/RXOV	SM2/TXCO	REN	TB8	RB8	TI	RI
SBUF	99H	Serial Data Buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADDR	9AH	Slave Address	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN	9BH	Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
SBRTH	9CH	Baud rate high byte	00000000	SBRTEN	SBRT0.14	SBRT0.13	SBRT0.12	SBRT0.11	SBRT0.10	SBRT0.9	SBRT0.8
SBRTL	9DH	Baud rate low byte	00000000	SBRT0.7	SBRT0.6	SBRT0.5	SBRT0.4	SBRT0.3	SBRT0.2	SBRT0.1	SBRT0.0
SFINE	9EH	Baud rate fine tuning for EUART0\1	00000000	SFINE.3	SFINE.2	SFINE.1	SFINE.0	SFINE.3	SFINE.2	SFINE.1	SFINE.0

Table 6.11 EUART1 SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power & serial Control	00000000	SMOD	SSTAT	SSTAT1	SIDL	GF1	GF0	PD	IDL
SCON1	D8H	Serial Control	00000000	SM10/FE1	SM11/RXO	SM12/TXC	REN1	TB18	RB18	TI1	RI1
SBUF1	D9H	Serial Data Buffer	00000000	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
SADDR1	DAH	Slave Address	00000000	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
SADEN1	DBH	Slave Address Mask	00000000	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
SBRT1H	DCH	Baud rate high byte	00000000	SBRTEN1	SBRT1.14	SBRT1.13	SBRT1.12	SBRT1.11	SBRT1.10	SBRT1.9	SBRT1.8
SBRT1L	DDH	Baud rate low byte	00000000	SBRT1.7	SBRT1.6	SBRT1.5	SBRT1.4	SBRT1.3	SBRT1.2	SBRT1.1	SBRT1.0
SFINE	9EH	Baud rate fine tuning for EUART0\1	00000000	SFINE.3	SFINE.2	SFINE.1	SFINE.0	SFINE.3	SFINE.2	SFINE.1	SFINE.0

Table 6.12 EUART3 SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON3	FFD0H	Serial Control	00000000	SM30	SM31	SM32	REN3	TB83	RB83	TI3	RI3
SBUF3	FFD1H	Serial Data Buffer	00000000	SBUF3.7	SBUF3.6	SBUF3.5	SBUF3.4	SBUF3.3	SBUF3.2	SBUF3.1	SBUF3.0
SADDR3	FFD2H	Slave Address	00000000	SADDR3.7	SADDR3.6	SADDR3.5	SADDR3.4	SADDR3.3	SADDR3.2	SADDR3.1	SADDR3.0
SADEN3	FFD3H	Slave Address Mask	00000000	SADEN3.7	SADEN3.6	SADEN3.5	SADEN3.4	SADEN3.3	SADEN3.2	SADEN3.1	SADEN3.0
SBRT3H	FFD4H	Baud rate high byte	00000000	SBRTEN3	SBRT3.14	SBRT3.13	SBRT3.12	SBRT3.11	SBRT3.10	SBRT3.9	SBRT3.8
SBRT3L	FFD5H	Baud rate low byte	00000000	SBRT3.7	SBRT3.6	SBRT3.5	SBRT3.4	SBRT3.3	SBRT3.2	SBRT3.1	SBRT3.0
SFINE2	DEH	Baud rate fine tuning for EUART	00000000	SFINE3.3	SFINE3.2	SFINE3.1	SFINE3.0	SFINE2.3	SFINE2.2	SFINE2.1	SFINE2.0

Table 6.15 IR SFR

Mnem	Addr	Name	POR/WDT /LVR/PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRCON1	ADH	IR control	00--0000	IRON	IRS	-	-	IRF11	IRF10	IRF9	IRF8
IRDAT	AEH	IR carrier frequency	00000000	IRF7	IRF6	IRF5	IRF4	IRF3	IRF2	IRF1	IRF0
IRCON2	AFH	IR control 2	------00	-	-	-	-	-	-	IRSEL1	IRSEL0

Table 6.16 ADC SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	C1H	ADC control	00000000	ADON	ADCIF	TPSCON	SCH3	SCH2	SCH1	SCH0	GO/$\overline{DONE}$
ADT	C2H	ADC Configuration mode	011---00	ADCCLK1	ADCCLK0	ADCM	-	-	-	CICCTL1	CICCTL0
ADCH	C3H	ADC channel control	00000000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
ADDL	C4H	ADC data low byte	00000000	A7	A6	A5	A4	A3	A2	A1	A0
ADDH	C5H	ADC data high byte	--000000	-	-	A13	A12	A11	A10	A9	A8

Table 6.17 LCD SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON2	D2H	LCD contrast control	0-000000	FCMOD	-	FCCTL1	FCCTL0	LCDLDOEN	MOD2	MOD1	MOD0
LCDCON1	D1H	LCD control	00000000	LCDON	DUTY2	DUTY1	DUTY0	BIAS	CONTR2	CONTR1	CONTR0
P4SS	FF80H	P4 or Segment Select	0000----	P4S7	P4S6	P4S5	P4S4	-	-	-	-
P5SS	FF81H	P5 or Segment Select	00000000	P5S7	P5S6	P5S5	P5S4	P5S3	P5S2	P5S1	P5S0
P6SS	FF82H	P6 or Segment Select	00000000	P6S7	P6S6	P6S5	P6S4	P6S3	P6S2	P6S1	P6S0
P7SS	FF83H	P7 or Segment Select	00000000	P7S7	P7S6	P7S5	P7S4	P7S3	P7S2	P7S1	P7S0
P8SS	FF84H	P8 or Segment Select	00000000	P8S7	P8S6	P8S8	P8S4	P8S3	P8S2	P8S1	P8S0
P9SS	FF85H	P9 or Segment Select	00000000	P9S7	P9S6	P9S9	P9S4	P9S3	P9S2	P9S1	P9S0

Table 6.18 RTC SFRs

Mnem	Addr	Name	POR	WDT/LVR/PINReset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBSC	FFA0H	Sub second REG	********	uuuuuuuu	SBSC7	SBSC6	SBSC5	SBSC4	SBSC3	SBSC2	SBSC1	SBSC0
SEC	FFA1H	Second REG	********	uuuuuuuu	-	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
MIN	FFA2H	Minute REG	-*******	-uuuuuuu	-	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
HR	FFA3H	Hour REG	--******	--uuuuuu	-	-	HR5	HR4	HR3	HR2	HR1	HR0
DAY	FFA4H	Date REG	--******	--uuuuuu	-	-	DAY5	DAY4	DAY3	DAY2	DAY1	DAY0
MTH	FFA5H	Month REG	---*****	---uuuuu	-	-	-	MTH4	MTH3	MTH2	MTH1	MTH0
YR	FFA6H	Year REG	********	uuuuuuuu	YR7	YR6	YR5	YR4	YR3	YR2	YR1	YR0
DOW	FFA7H	Day REG	-----***	-----uuu	-	-	-	-	-	DOW2	DOW1	DOW0
RTCDATH	FFA8H	RTC compensation value (E) high byte	--******	--uuuuuu	-	-	E13	E12	E11	E10	E9	E8
RTCDATL	FFA9H	RTC compensation value (E) low byte	********	uuuuuuuu	E7	E6	E5	E4	E3	E2	E1	E0
RTCALM	FFAAH	RTC alarmer control	********	uuuuuuuu	ALM1C2	ALM1C1	ALM1C0	ALM0C4	ALM0C3	ALM0C2	ALM0C1	ALM0C0
A0SEC	FFABH	Alarmer0 Second REG	-*******	-uuuuuuu	-	A0SEC6	A0SEC5	A0SEC4	A0SEC3	A0SEC2	A0SEC1	A0SEC0
A0MIN	FFACH	Alarmer0 Minute REG	-*******	-uuuuuuu	-	A0MIN6	A0MIN5	A0MIN4	A0MIN3	A0MIN2	A0MIN1	A0MIN0
A0HR	FFADH	Alarmer0 Hour REG	--******	--uuuuuu	-	-	A0HR5	A0HR4	A0HR3	A0HR2	A0HR1	A0HR0
A0DAY	FFAEH	Alarmer0 Date REG	--******	--uuuuuu	-	-	A0DAY5	A0DAY4	A0DAY3	A0DAY2	A0DAY1	A0DAY0
A0DOW	FFAFH	Alarmer0 Day REG	-----***	-----uuu	-	-	-	-	-	A0DOW2	A0DOW1	A0DOW0
A1SEC	FFB0H	Alarmer1 Second REG	-*******	-uuuuuuu	-	A1SEC6	A1SEC5	A1SEC4	A1SEC3	A1SEC2	A1SEC1	A1SEC0
A1MIN	FFB1H	Alarmer1 Minute REG	-*******	-uuuuuuu	-	A1MIN6	A1MIN5	A1MIN4	A1MIN3	A1MIN2	A1MIN1	A1MIN0
A1HR	FFB2H	Alarmer1 Hour REG	--******	--uuuuuu	-	-	A1HR5	A1HR4	A1HR3	A1HR2	A1HR1	A1HR0
RTCCON	FFB3H	RTC control	0***00**	0uuuuuuu	RTCRD	ITEN	ITS1	ITS0	OUTEN1	OUTEN0	OUTS	OUTF
RTCWR	FFB4H	Writtern protect for RTC	00000000	00000000	RTCWR7	RTCWR6	RTCWR5	RTCWR4	RTCWR3	RTCWR2	RTCWR1	RTCWR0
RTCPSW	FFB5H	Writtern protect security code for RTC	00000000	00000000	PSW7	PSW6	PSW5	PSW4	PSW3	PSW2	PSW1	PSW0
RTCIE	FFB6H	RTC interrupt control	0000000	00000000	IT0IE	DAYIE	HRIE	MINIE	SECIE	ALM1IE	ALM0IE	-
RTCIF	FFB7H	RTC interrupt flag	*******-	uuuuuuu-	IT0IF	DAYIF	HRIF	MINIF	SECIF	ALM1IF	ALM0IF	-
RTCECL	FFB8H	RTC bias at room temperature low byte	uuuuuuuu	uuuuuuuu	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
RTCECH	FFB9H	RTC bias at room temperature high byte	uuuuuuuu	uuuuuuuu	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8
RTCTMR	FFBAH	RTC Timer	uuuuuuu	uuuuuuuu	RTCT.7	RTCT.6	RTCT.5	RTCT.4	RTCT.3	RTCT.2	RTCT.1	RTCT.0

Note: u：Reset does not affect the current value；*：Power on reset value is random number, and other forms of reset is u.

Table 6.19 EMU SFRs

Mnem	Addr	Name	POR/WDT/LVR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EADR	91H	EMU Address Register	00000000	RW	EADR.6	EADR.5	EADR.4	EADR.3	EADR.2	EADR.1	EADR.0
EDTAH	92H	EMU Data Register high byte	00000000	EDTAH.7	EDTAH.6	EDTAH.5	EDTAH.4	EDTAH.3	EDTAH.2	EDTAH.1	EDTAH.0
EDTAM	93H	EMU Data Register mid byte	00000000	EDTAM.7	EDTAM.6	EDTAM.5	EDTAM.4	EDTAM.3	EDTAM.2	EDTAM.1	EDTAM.0
EDTAL	94H	EMU Data Register low byte	00000000	EDTAL.7	EDTAL.6	EDTAL.5	EDTAL.4	EDTAL.3	EDTAL.2	EDTAL.1	EDTAL.0
EMUSR	95H	EMU Status/Control Register	********	DSPEN	EMUCLKS1	EMUCLKS0	SAGF	NoQLd	NoPLd	REVQ	REVP
EMUIE	96H	EMU interrupt enable Register	00000000	RMTEIE	DIMIE	DSPIE	QFIE	PFIE	SAMIE	SAGIE	ZXIE
EMUIF	97H	EMU interrupt request Register	00000000	RMTEIF	DIMIF	DSPIF	QFIF	PFIF	SAMIF	SAGIF	ZXIF

Note: EMUSR initial value will vary according to the different types of reset.

SFR mapping figure

	Bit Addressable	Non Bit Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	SCON2	SBUF2	SADDR2	SADEN2	SBRT2H	SBRT2L	OSCLO	(Reserved)	FFh
F0h	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7h
E8h	EXF0	P5	P6	P7	P8	P9	IB_OFFSET	IB_DATA	EFh
E0h	ACC	TK0L	TK0H	TK1L	TK1H	TK2L	TK2H	PASLO	E7h
D8h	SCON1	SBUF1	SADDR1	SADEN1	SBRT1H	SBRT1L	SFINE2	TK2BASEH	DFh
D0h	PSW	LCDCON1	LCDCON2	TK0BASEL	TK0BASEH	TK1BASEL	TK1BASEH	TK2BASEL	D7h
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		TK0DIFL	CFh
C0h	P4	ADCON	ADT	ADCH	ADCDL	ADCDH	LPDCON1	LPDCON2	C7h
B8h	IPL0	IPL1	IPH0	IPH1	TK0DIFH	TK1DIFL	TK1DIFH	TK2DIFL	BFh
B0h	P3	RSTSTAT	CLKCON	PWRCON1	PWRCON2	LDOCON	PBANK	PBANKLO	B7h
A8h	IEN0	IEN1	IENX	EXCON1	EXCON2	IRCON1	IRDAT	IRCON2	AFh
A0h	P2	SPCON	SPSTA	SPDAT	TKCON	TK2DIFH	TKF0	FLASHCON	A7h
98h	SCON	SBUF	SADDR	SADEN	SBRTH	SBRTL	SFINE	PWMCON	9Fh
90h	P1	EADR	EDTAH	EDTAM	EDTAL	EMUSR	EMUIE	EMUIF	97h
88h	TCON	TMOD	TL0	TL1	TH0	TH1	SUSLO	TCON1	8Fh
80h	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

	Non Bit Addressable								
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
FFF8h	P8PCR	P9PCR	P0INM	P2INM					FFFFh
FFF0h	P0PCR	P1PCR	P2PCR	P3PCR	P4PCR	P5PCR	P6PCR	P7PCR	FFF7h
FFE8h	P8CR	P9CR							FFEFh
FFE0h	P0CR	P1CR	P2CR	P3CR	P4CR	P5CR	P6CR	P7CR	FFE7h
FFD8h									FFDFh
FFD0h	SCON3	SBUF3	SADDR3	SADEN3	SBRT3H	SBRT3L			FFD7h
FFC8h	RXBUF	TXBUF	S7816IE	S7816STA	S7816ERRSTA	EGTRSEND			FFCFh
FFC0h	S7816EN	S7816CON	EGTSET	S7816WTH	S7816WTL	S7816CLKDIV	S7816ETUH	S7816ETUL	FFC7h
FFB8h	RTCECL	RTCECH	RTCTMR	-	-	-	-	-	FFBFh
FFB0h	A1SEC	A1MIN	A1HR	RTCCON	RTCWR	RTCPSW	RTCIE	RTCIF	FFB7h
FFA8h	RTCDATH	RTCDATL	RTCALM	A0SEC	A0MIN	A0HR	A0DAY	A0DOW	FFAFh
FFA0h	SBSC	SEC	MIN	HR	DAY	MTH	YR	DOW	FFA7h
FF98h			TKST	TKRANDOM	TKDIV01	TKDIV02	TKDIV03	TKDIV04	FF9Fh
FF90h	TKVREF	TKCH	TK0THRL	TK0THRH	TK1THRL	TK1THRH	TK2THRL	TK2THRH	FF97h
FF88h	P0OS	P2OS	P3OS	P0DRVH	P1DRVL	P2DRVH	P0PHM	P2PHM	FF8Fh
FF80h	P4SS	P5SS	P6SS	P7SS	P8SS	P9SS			FF87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

note: The unused addresses of SFR are not available.

SFR Reset Value

SFR Name	Reset Value
ACC	00000000b
B	00000000b
AUXC	00000000b
PSW	00000000b
SP	00000111b
DPL	00000000b
DPH	00000000b
DPL1	00000000b
DPH1	00000000b
INSCON	00000000b

7.Normal Function

7.1 CPU

7.1.1 CPU Core SFR

Feature

CPU core registers:ACC，B，PSW，SP，DPL，DPH

Accumulator

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET,RETI executions. The stack may reside anywhere in on-chip internal RAM（00H-FFH）. On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Table 7.2 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	CY	Carry flag bit 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	AC	Auxiliary Carry flag bit 0: an auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	F0	F0 flag bit Available to the user for general purposes
4-3	RS[1:0]	R0-R7 Register bank select bits 00: Bank 0 (Address to 00H-07H) 01: Bank 1 (Address to 08H-0FH) 10: Bank 2 (Address to 10H-17H) 11: Bank 3 (Address to 18H-1FH)
2	OV	Overflow flag bit 0: no overflow happen 1: an overflow happen
1	F1	F1 flag bit Available to the user for general purposes
0	P	Parity flag bit 0: an even number of ``one'' bits in the Accumulator 1: an odd number of ``one'' bits in the Accumulator

Data Pointer Register（DPTR）

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

7.1.2 Enhanced CPU core SFRs

Extended 'MUL' and 'DIV' instructions: 16bit*8bit, 16bit/8bit
Dual Data Pointer
Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON
The G80F975A has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8 bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16 bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8 bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16 bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer
Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is the same with DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

7.1.3 Register

Table 6.3 Data Pointer Select Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	-	-	-	-	DIV	MUL	-	DPS
R/W	-	-	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	-	0

Bit Number	Bit Mnemonic	Description
3	DIV	16 bit / 8 bit Divide Selection Bit 0: 8 bit Divide 1: 16 bit Divide
2	MUL	16 bit / 8 bit Multiply Selection Bit 0: 8 bit Multiply 1: 16 bit Multiply
0	DPS	Data Pointer Selection Bit 0: Data pointer 1: Data pointer1

7.2 RAM

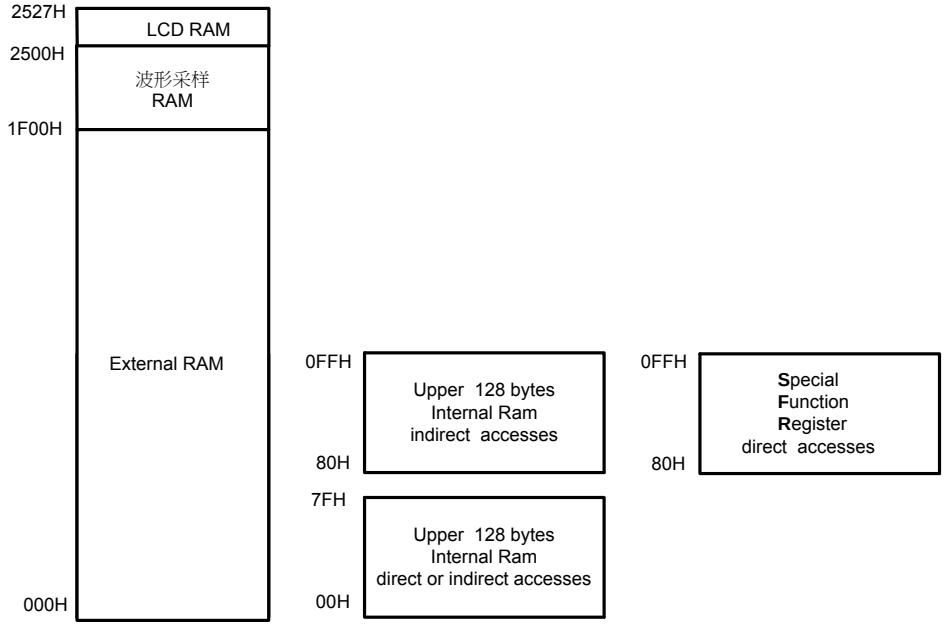
7.2.1 Features

The G80F975A provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:
1. The Lower 128 bytes of RAM (addresses 00h to 7Fh) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80h to FFh) are indirectly addressable only.
3. The Special Function Registers (SFR, addresses 80h to FFh) are directly addressable only.
4. The expanded RAM bytes are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7Fh, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.
Note: the unused address is unavailable in SFR.

The G80F975A provides additional 7936 bytes RAM in external data space for increasing data handling requirement, high level language support and LCD RAM (2500H – 2527H) configuration. And the measurement waveform sampling RAM(1F00H~24FFH).

The Internal and External RAM configuration



Internal and External RAM Address

The G80F975A provides traditional method for accessing of external RAM. Use MOVX A, @Ri or MOVX @Ri, A; to access external low 256 bytes RAM; MOVX A, @DPTR or MOVX @DPTR, A to access external 64K bytes RAM.

In G80F975A , the user can also use XPAGE register to access external RAM only with MOVXA, @Ri or MOVX @Ri, A instructions. The user can use XPAGE to represent the high byte address of RAM above 256 Bytes.

In flash SSP mode, the XPAGE can also be used as sector selector (Refer to SSP Function)

7.2.2 Register

Table 6.4 Data memory page Register

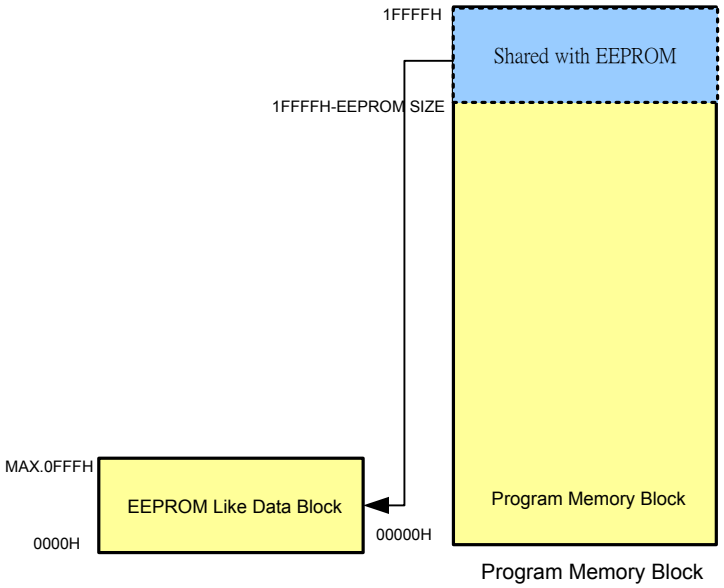
F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	XPAGE[7:0]	RAM Page Selector

7.3 Flash Program Memory

7.3.1 Features

The program memory consists256 X 512B sectors, total 128KB
Flash memory includes 256 X 512 b block, a total of 128 KB
largest block 4 k class EEPROM storage area (the option to choose)
Programming and erase can be done over the full operation voltage range
Support 4 code protection mode
Write, read and erase operation are all supported by In-Circuit Programming (ICP)
Support overall/sector erase and programming
Minimum program/erase cycles: Program block :100，000
EEPROM-like block ：100，000
Minimum years data retention: 20
Low power consumption



Program Memory Block

The G80F975A embeds 128K flash program memory for program code. The flash program memory provides electrical erase and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode. Every sector is 512 bytes.

The built-in page switching technique is used to extend the CPU address range.The first 32K image of the CPU address space is the low 32K (BANK0) of the Flash space.The high 32K image of the CPU address space is 4 pages.

As shown below:

CPU Addr	ROM space			
	BANK = $00	BANK = $01	BANK = $02	BANK = $03
$0000 - $7FFF	00000 – 07FFF （BANK 0）	00000 - 07FFF （BANK 0）	00000 - 07FFF （BANK 0）	00000 - 07FFF （BANK 0）
$8000 - $FFFF	00000 – 07FFF （BANK 0）	08000 – 0FFFF （BANK 1）	10000 – 17FFF （BANK 2）	18000 - 1FFFF （BANK 3）

The G80F975A also embeds 4096 bytes EEPROM-like memory block for storing user data. Every sector is 512 bytes. It has 8 sectors
It is important to note that the storage code area and EEPROM storage area share 128K FLASH.The EEPROM size is determined by OP_EEPROMSIZE[3:0].
Flash operation definition:
In-Circuit Programming (ICP): Through the Flash programmer to wipe the Flash memory, read and write operations.

Self-Sector Programming (SSP) mode: User Program code run in Program Memory to wipe the Flash memory, read and write operations. But it can not erase the sector which contains program itself.

Flash Memory Supports the Following Operations:
(1) Code Protection Control Mode
G80F975A code protection function provides a high-performance security measures for the user. It provided 4 protection modes in total.
Code protection mode 0: encrypt the programmer, allow/forbid any programmer write/read operations (not including overall erase), the uint is 4K (8 sectors), and can protect them respectively.
Code protection mode 1: encrypt the MOVC instruction, allow/forbid through MOVC instructions to read operation in other sectors, or through SSP mode to erased/write operation, the uint is 4K (8 sectors), and can protect them respectively.◦
Code protection mode 2: SSP function allow/forbid control, when selected, chip's SSP operation (erase or write, not include read)for code block is forbid, but not for EEPROM-like.
Code protection mode 3: customer password protection, can set password by customer, the password is 6 bytes. If this function is enable, it means that entering this password first before the programmer or simulator tool do any operation (read, write, erase or simulate)for the chip, if the password is right, then the chip allows the programmer or simulator tool to do the corresponding operation, otherwise it gives error, and don't perform the corresponding operation.
The user must use one of the following two ways to complete code protection control mode Settings:
I. Flash programmer in ICP mode is set to corresponding protection bit to enter the protected mode.
II. The SSP mode does not support code protection control mode programming.
(2) Overall Erase
Regardless of the state of the code protection control mode, the overall erase operation will erase all programs, code options, the code protection bit, but they will not erase EEPROM-like memory block.
The user must use the following way to complete the overall erase:
1.Flash programmer in ICP mode send overall erase instruction to run overall erase.
2.The SSP mode does not support overall erase mode.
(3) Sector Erase
Sector erase operations will erase the content of selected sector. The user program (SSP) and Flash programmer can perform this operation.
For user programs to perform the operation, code protection mode 1and mode 2 in the selected sector must be forbidden.
For Flash programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden. If code protection mode 3 is enable, user must enter the correct password.
The user must use one of the following two ways to complete sector erase:
1. Flash programmer in ICP mode send sector erase instruction to run sector erase.
2. Through the SSP function send sector erase instruction to run sector erase (see chapter SSP).
(4) EEPROM-like Memory Block Erase
EEPROM-like memory block erase operations will erase the content in EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.
The user must use one of the following two ways to complete EEPROM-like memory block erase:
1. Flash programmer in ICP mode send EEPROM-like memory block erase instruction to run EEPROM-like memory block erase.
2. Through the SSP function send EEPROM-like memory block erase instruction to run EEPROM-like memory block erase (see chapter SSP).
(5) Write/Read Code
Write/read code operation can read or write code from flash memory block. The user program (SSP) and Flash programmer can perform this operation.

For user programs to perform the reading operation, code protection mode 1in the selected sector must be forbidden. Regardless of the security bit Settings or not, the user program can read/write the sector which contains program itself (the unit is 512Byte).
For Flash programmer to perform the writting operation, code protection mode 1 and mode 2 in the selected sector must be forbidden.

Note: If only enable code protection control mode 1, the user program can't write other sectors, but it can write the sector which contains program itself (the unit is 1K).
If use the programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden.

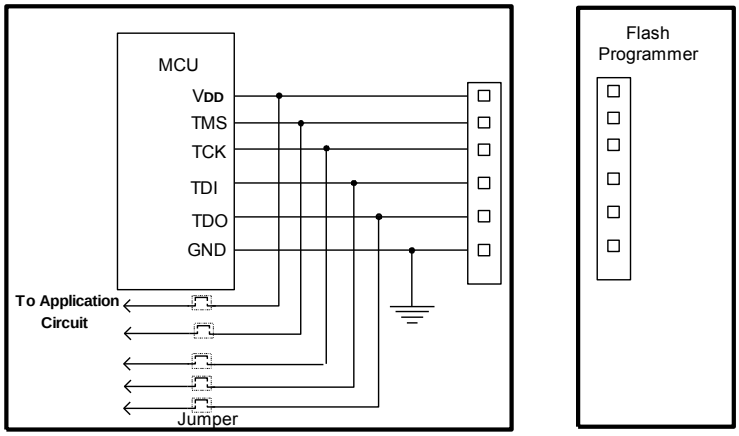
(6) Write/Read EEPROM-like Memory Block
EEPROM-like memory block operation can read or write data from EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.
The user must use one of the following two ways to complete write/read EEPROM-like memory block:
1. Flash programmer in ICP mode send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.
2. Through the SSP function send write/read EEPROM-like memory block instruction to run write EEPROM-like memory block; Through MOVC instruction to perform reading EEPROM-like operation.

Flash Memory Block Operation Summary

Operation	ICP	SSP
Code Protection	support	not support
Sector Erase	support (no security bit)	support (no security bit)
Overall Erase	support	not support
EEPROM-like memory block erase	support	support
Write/Read	support (no security bit)	support (no security bit)
Read/write EEPROM-like memory block	support	support

7.3.2 Flash Operation in ICP Mode

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 wires (VDD, GND, TCK, TDI, TMS, TDO).
At first the four JTAG pins (TDO, TDI, TCK, TMS) are used to enter the programming mode. Only after the three pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the FLASH Programmer's user guide.
In ICP mode，all the flash operations are completed by the programmer through 6-wire interface. Since the program timing is very sensitive, 6 jumpers are needed (VDD, GND, TDO, TDI, TCK, TMS) to separate the program pins from the application circuit as the following diagram.



The recommended steps are as following:
(1) The jumpers must be open to separate the programming pins from the application circuit before programming.
(2) Connect the programming interface with programmer and begin programming.
(3) Disconnect programmer and short these jumpers after programming is complete.

7.4 SSP Function

The G80F975A provides SSP (Self Sector Programming) function, each sector can be sector erased or programmed by the user's code if the selected sector is not be protected. But once sector has been programmed, it cannot be reprogrammed before sector erase.

The G80F975A build in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON2~5), the SSP will be terminated.

7.4.1 Registers

Table 7.4 BANK Lock Registers

B7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PBANKLO	PBANKLO.7	PBANKLO.6	PBANKLO.5	PBANKLO.4	PBANKLO.3	PBANKLO.2	PBANKLO.1	PBANKLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （POR/WDT/LVR/PIN）	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PBANKLO[7：0]	PBANK Lock Registers Any write action to the RegistersPBANK is invalid when the PBANKLORegisters are not 55H.

Table 7.5 BANK Switch Registers

B6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PBANK	-	-	COBANK.1	COBANK.0	-	-	IFBANK.1	IFBANK.0
R/W	-	-	R/W	R/W	-	-	R/W	R/W
Reset Value （POR/WDT/LVR/PIN）	-	-	0	1	-	-	0	1

Bit Number	Bit Mnemonic	Description
5-4	COBANK[1：0]	Target data address (Constant Operations Target) BANK switching position. 00：Target data location BANK0 01：Target data location BANK1 10：Target data location BANK2 11：Target data location BANK3
1-0	IFBANK[1：0]	Take the Instruction Fetch Operation. 00：command BANK0 01：command BANK1 10：command BANK2 11：command BANK3

Sector select Register for erase/programming and Offset register for Programming

This register is used to select the block code of the sector to be erased/programmed, and coordinates IB_OFFSET register to indicate the address offset of the byte to be programmed in sector.

For program memory, one sector is 512 bytes, register is defined as follows:

Table 7.6 Offset register for programming

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-1	XPAGE[7:1]	Sector of the flash memory to be programmed, 000000---means sector 0, and so on
0	XPAGE0	High Address of Offset of the flash memory sector to be programmed

Table 7.7 Offset of flash memory for programming

EEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFFSET.7	IB_OFFSET.6	IB_OFFSET.5	IB_OFFSET.4	IB_OFFSET.3	IB_OFFSET.2	IB_OFFSET.1	IB_OFFSET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	IB_OFFSET[7:0]	Low Address of Offset of the flash memory sector to be programmed

XPAGE0 and IB_OFFSET[7:0] are 9 bits in total, can indicate the offset of all 512 bytes in 1 program memory block.
EEPROM-like sectors, one sector is 512 bytes, in total 8 sectors, register is defined as follows:

Table 7.8 Sector select Register for erase/programming

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	XPAGE.7	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-4	XPAGE[7:4]	No significance at the time erase/programming sector
3-1	XPAGE[3:1]	Erased/programmed sector select bit 000：sector 0 001：sector 1 … 111: sector 7
0	XPAGE0	The high address of the storage unit that is erased/programmed.

Use “MOVC A, @A+DPTR” or “MOVC A, @A+PC” to access EEPROM-like sectors.
Note: Need to set FAC bit in FLASHCON register.

Table 7.9 Offset register for Programming

EEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFFSET.7	IB_OFFSET.6	IB_OFFSET.5	IB_OFFSET.4	IB_OFFSET.3	IB_OFFSET.2	IB_OFFSET.1	IB_OFFSET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	IB_OFFSET[7:0]	Erased/programmed block unit address

IB_OFFSET[7:0] are 8bits in total, can indicate the offset of all 256 bytes in 1 block.

Table 7.10 Data Register for Programming

EFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	IB_DATA[7:0]	Data to be programmed

Table 7.11 Type select Registe

F2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	IB_CON1[7:0]	Type select ： 0xE6: Sector Erase 0x6E: Sector Programming

Table 7.12 SSP Flow Control Register1

F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	IB_CON2[3:0]	Must be 05H, else Flash Programming will terminate

Table 7.13 SSP Flow Control Register2

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	IB_CON3[3:0]	Must be 0AH else Flash Programming will terminate

Table 7.14 SSP Flow Control Register3

F5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

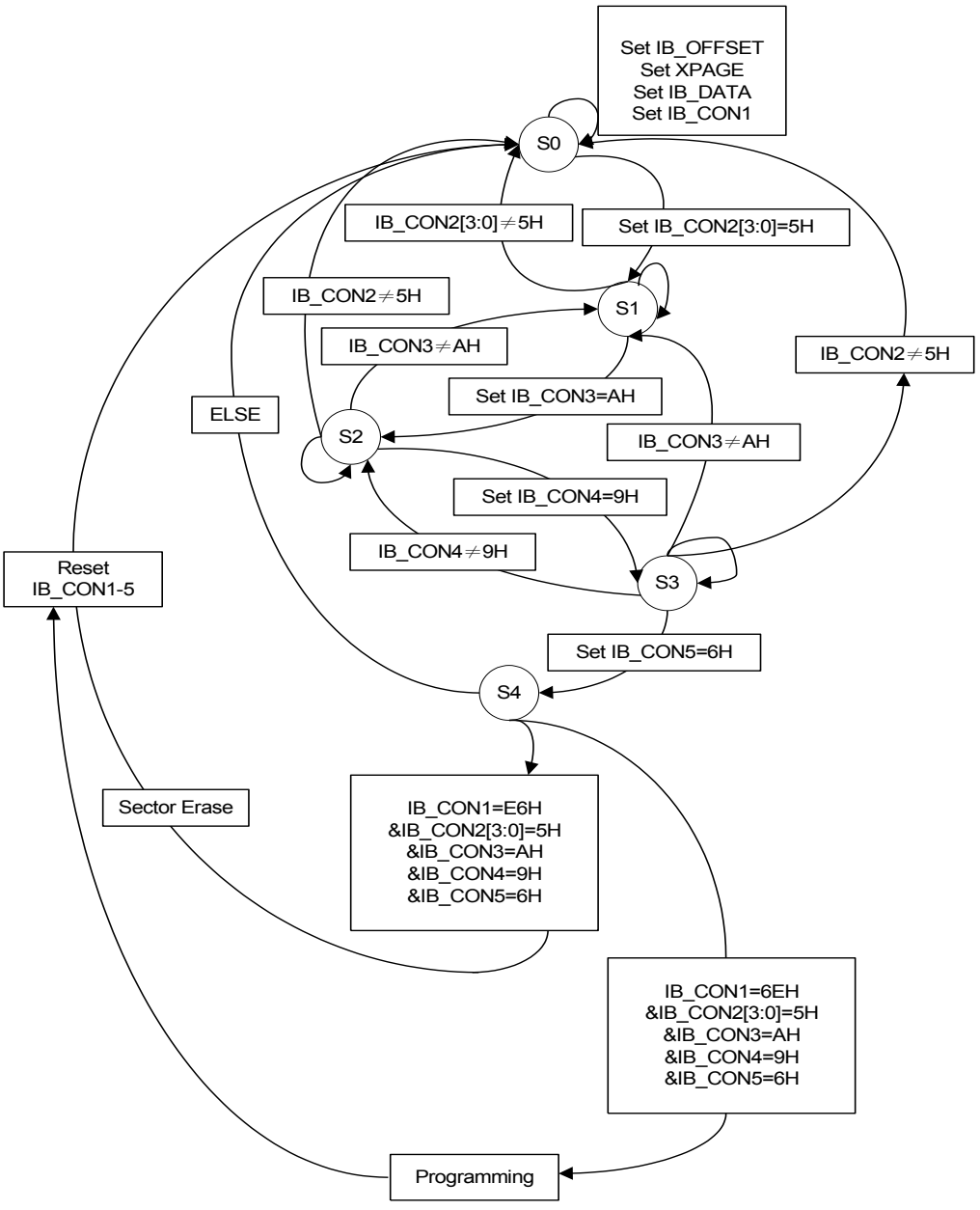
Bit Number	Bit Mnemonic	Description
3-0	IB_CON4[3:0]	Must be 09H, else Flash Programming will terminate

Table 7.15 SSP Flow Control Register4

F6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	IB_CON5[3:0]	Must be 06H, else Flash Programming will terminate

7.4.2 Flash Control Flow



7.4.3 SSP Programming Notice

To successfully complete SSP programming, the user's software must following the steps below:

A. For Code/Data Programming: note: need to close code protection mode 1 and mode 2
1. Disable interrupt;
2. Fill in the XPAGE, IB_OFFSET for the corresponding address;
3. Fill in IB_DATA if programming is wanted;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Code/Data programming, CPU will be in IDLE mode; Exit IDLE mode automatically after programming;
7. Go to Step 2 if more data are to be programmed;
8. Clear XPAGE; enable interrupt if necessary.

B. For Sector Erase:
1. Disable interrupt;
2. Fill in the XPAGE for the corresponding sector;
3. Fill in IB_CON1-5 sequentially;
4. Add 4 NOPs for more stable operation;
5. Sector Erase, CPU will be in IDLE mode; Exit IDLE mode automatically after programming;
6. Go to step 2 if more sectors are to be erased;
7. Clear XPAGE; enable interrupt if necessary.

C. For Code Reading:
Just Use "MOVC A, @A+DPTR" or "MOVC A, @A+PC".

D. For EEPROM-Like:
Steps is same as code programming, the differences are:
1. Set FAC bit in FLASHCON register before programming or erase EEPROM-Like;
2. One sector of EEPROM-Like is 256 bytes, not 1024 bytes.

Note:The FAC bit must be cleared if not need to operate EEPROM-Like.

7.4.4 Readable identification code

Each G80F975A chip were cured a 40bits readable identification code after the factory. Its value is a random value between 0 - 0xFFFFFFFFFF and unable to be erased, and can be read by program or programming tools.

For example：
```
Unsigned char Temp1，Temp2，Temp3，Temp4，Temp5;
FLASHCON = 0x01;
Temp1 = CBYTE[0x127b];
Temp2 = CBYTE[0x127c];
Temp3 = CBYTE[0x127d];
Temp4 = CBYTE[0x127e];
Temp5 = CBYTE[0x127f];
FLASHCON = 0x00;
```

Note: The FAC bit must be cleared after reading readable identification code, otherwise it will effect the instruction execution of user's program

FLASHCON register description is as follows:：

Table 7.16 Flash Access Control Register

A7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FLASHCON	-	-	-	-	-	-	-	FAC
R/W	-	-	-	-	-	-	-	R/W
Reset Value(POR/WDT/LVR)	-	-	-	-	-	-	-	0

Bit Number	Bit Mnemonic	Description

0	FAC	FAC: Flash access control 0: MOVC or SSP access main memory 1: MOVC or SSP access EEPROM-like

7.5 System Clock and Oscillator

7.5.1 Features

Only support 1 oscillator type: 32.768kHz crystal
Built-in temperature linear 32 KHz low-frequency RC oscillator.
Built-in phase locked loop (PLL) oscillator
Built-in 8 MHz high frequency RC oscillator.
Built-in 32.768kHz speed up circuit
Built-in system clock prescaler

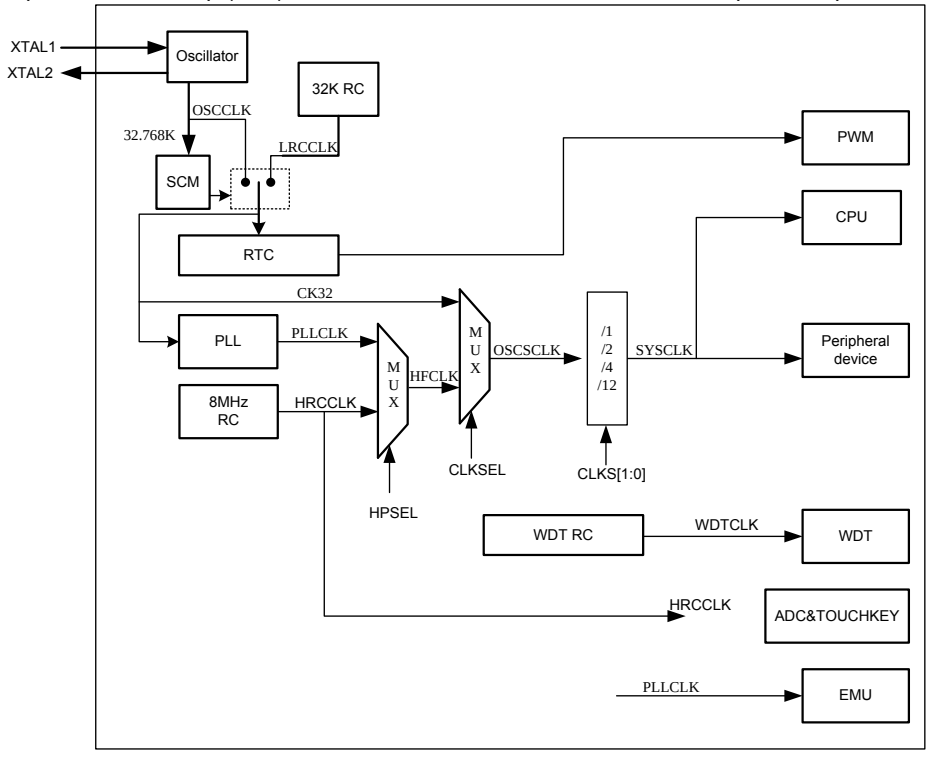
7.5.2 Clock definition

The G80F975A have several internal clocks defined as below:

OSCCLK: the oscillator clock is 32.768kHz crystal.
fOSC is defined as the OSCCLK frequency. tOSC is defined as the OSCCLK period.
LRCCLK：Internal 32 KHz RC oscillator clock.FLRC is defined as the frequency of LRCCLK.TLRC is defined as the period of LRCCLK.
HRCCLK：Internal 8MHz RC oscillator clock.FHRC is defined as the frequency of HRCCLK.TLRC is defined as the period of HRCCLK.
PLLCLK: the PLL oscillator clock. fPLL is defined as the PLLCLK frequency. tPLL is defined as the PLLCLK period.
WDTCLK: the internal 2kHz WDT RC clock. fWDT is defined as the WDTCLK frequency. tWDT is defined as the WDTCLK period.
OSCSCLK: the input of system clock prescaler. It can be OSCCLK,LRCCLK,HRCCLK,PLLCLK clock. fOSCS is defined as the OSCSCLK frequency. tOSCS is defined as the OSCSCLK period.
SYSCLK: system clock, the output of system clock prescaler. It is the CPU instruction clock. fSYS is defined as the SYSCLK frequency. tSYS is defined as the SYSCLK period.

7.5.3 Description

G80F975A adopts double oscillator system architecture, the high frequency oscillator supports two types of oscillator: internal RC oscillator (8 MHZ), low frequency oscillator using the built-in 32 k RC oscillator and 32.768 KHz crystal resonator.The oscillator generates the basic clock pulse that provides the system clock to supply CPU and on-chip peripherals.
A phase locked loop (PLL) oscillator is built in G80F975A, which can provide up to 9.8304MHz oscillator clock.



7.5.4 Registers

Table 7.17 System Clock Control register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	32K_SPDUP	CLKS1	CLKS0	SCMF	HFON	CLKSEL	PLLSEL	HFSEL
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	1	1	1	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	32K_SPDUP	32.768kHz oscillator speed up mode control bit 0: 32.768kHz oscillator normal mode, cleared by software. 1: 32.768kHz oscillator speed up mode, set by hardware or software. This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. And this bit also can be set or cleared by software if necessary. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption
6-5	CLKS[1:0]	SYSCLK Prescaler Register 00：fSYS = fOSCS 01：fSYS = fOSCS/2 10：fSYS = fOSCS/4 11：fSYS = fOSCS/12 If 32.768kHz oscillator is selected as OSCSCLK, these control bits is invalid.
4	SCMF	Stop vibration detection of 32K crystal oscillator (OSCCLK) 0：The hardware clear 0 indicates that the 32K oscillator is normal and CK32 is provided by the 32.768 oscillator. 1：The hardware set 1 represents the stop vibration of 32K oscillator, and CK32 is provided by the 32K RC oscillator.
3	HFON	High frequency clock enables energy level. 0: Close all high frequency clocks. 1: The high frequency clock is turned on, and PLL or 8MHz RC is determined by HFSEL.
2	CLKSEL	Frequency Select Register 0: 3CK32is selected as OSCSCLK. 1: HFCLK is selected as OSCSCLK.
1	PLLSEL	PLLOscillator frequency Registers 0:30 times frequency 1: invalid operation
0	HFSEL	High frequency clock selection: 0: select PLL as the high frequency clock source. 1: select 8M RC as the high frequency clock source.

Note:

To select PLLCLK as OSCSCLK, the steps below must be done in sequence:

(1) Set the selection of PLL frequency, PLLSEL=0.

(2) Set high frequency clock selection, HFSEL= 0.

(3) Set HFON =1 and turn on the PLL oscillator

(4) Wait at least 5ms

(5) Set CLKSEL =1 to select HFCLK as OSCSCLK

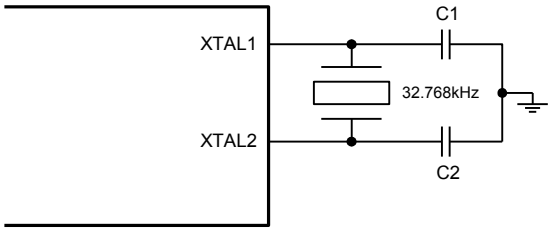
When the system clock is switched between PLL and 8MHz RC oscillator, the system needs to be switched to CK32 first.

Table 7.18 System clock lock RegistersRegisters

FEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OSCLO	OSCLO.7	OSCLO.6	OSCLO.5	OSCLO.4	OSCLO.3	OSCLO.2	OSCLO.1	OSCLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （POR/WDT/LVR/PIN）	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	OSCLO[7：0]	System clock lock Registers When the OSCLORegisters are not 55H, any write to RegistersCLKCON is invalid.

7.5.5 Oscillator Type
32768Hz crystal&internal PLL :



Crystal Oscillator Frequency	Recommend Type	Manufacturer
32.768kHz	DT 38 (φ 3x8)	KDS
	φ 3x8 - 32.768kHz	Shenzhen DGJB Electronic Co.,Ltd.

Notes:
(1) Capacitor values are used for design guidance only!
(2) These capacitors were tested with the crystals listed above for basic start-up and operation. They are not optimized.
(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected VDD and the temperature range for the application.

7.6 I/O Port

7.6.1 Features

10 47-bit bi-directional I/O ports
Share with alternative functions

The G80F975A has 10 47-bit bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x=0-9,y=0-7).

G80F975A I/O ports are supplied by VOUT.

For G80F975A, some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions be conflict when all the functions are enabled. (Refer to Port Share Section for details)

7.6.2 Registers

Table 7.19 Port Control Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CR (FFE0H)	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR (FFE1H)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR (FFE2H)	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR (FFE3H)	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR (FFE4H)	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR (FFE5H)	P5CR.7	P5CR.6	P5CR.5	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P6CR (FFE6H)	P6CR.7	P6CR.6	P6CR.5	P6CR.4	P6CR.3	P6CR.2	P6CR.1	P6CR.0
P7CR (FFE7H)	P7CR.7	P7CR.6	P7CR.5	P7CR.4	P7CR.3	P7CR.2	P7CR.1	P7CR.0
P8CR (FFE8H)	P8CR.7	P8CR.6	P8CR.5	P8CR.4	P8CR.3	P8CR.2	P8CR.1	P8CR.0
P9CR (FFE9H)	P9CR.7	P9CR.6	P9CR.5	P9CR.4	P9CR.3	P9CR.2	P9CR.1	P9CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PxCRy x = 0-9, y = 0-7	Port input/output direction control Register 0: input mode (default) 1: output mode

Table 7.20 Port Pull up Resistor Control Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PCR (FFF0H)	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR (FFF1H)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR (FFF2H)	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR (FFF3H)	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR (FFF4H)	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR (FFF5H)	P5PCR.7	P5PCR.6	P5PCR.5	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
P6PCR (FFF6H)	P6PCR.7	P6PCR.6	P6PCR.5	P6PCR.4	P6PCR.3	P6PCR.2	P6PCR.1	P6PCR.0
P7PCR (FFF7H)	P7PCR.7	P7PCR.6	P7PCR.5	P7PCR.4	P7PCR.3	P7PCR.2	P7PCR.1	P7PCR.0
P8PCR (FFF8H)	P8PCR.7	P8PCR.6	P8PCR.5	P8PCR.4	P8PCR.3	P8PCR.2	P8PCR.1	P8PCR.0
P9PCR (FFF9H)	P9PCR.7	P9PCR.6	P9PCR.5	P9PCR.4	P9PCR.3	P9PCR.2	P9PCR.1	P9PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PxPCRy x = 0-9, y = 0-7	Input Port internal pull-high resistor enable/disable control 0: internal pull-high resistor disabled (default) 1: internal pull-high resistor enabled

Table 7.21 Port Data Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0 (80H)	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1 (90H)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2 (A0H)	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3 (B0H)	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4 (C0H)	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5 (E9H)	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0
P6 (EAH)	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0
P7 (EBH)	P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0
P8 (ECH)	P8.7	P8.6	P8.5	P8.4	P8.3	P8.2	P8.1	P8.0
P9 (EDH)	P9.7	P9.6	P9.5	P9.4	P9.3	P9.2	P9.1	P9.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	Px.y x = 0-9, y = 0-7	Port Data Register

Table 7.22 Port Output Mode Select Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0OS (FF88H)	P0OS.7	P0OS.6	P0OS.5	P0OS.4	P0OS.3	P0OS.2	P0OS.1	P0OS.0
P2OS (FF89H)	P1OS.7	P1OS.6	P1OS.5	P1OS.4	P1OS.3	P1OS.2	P1OS.1	P1OS.0
P3OS (FF8AH)	P2OS.7	P2OS.6	P2OS.5	P2OS.4	P2OS.3	P2OS.2	P2OS.1	P2OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PxOS.y x = 0,2,3, y = 0-7	port output mode selection 0：The pin output mode is N channel opening leakage output. 1：The pin output mode is CMOS pull output.

Table 7.23 Port output capability selection Registers

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0DRVH(FF8BH)	P0DH.7	P0DH.6	P0DH.5	P0DH.4	P0DH.3	P0DH.2	P0DH.1	P0DH.0
P2DRVH(FF8CH)	P2DH.7	P2DH.6	P2DH.5	P2DH.4	P2DH.3	P2DH.2	P2DH.1	P2DH.0
P1DRVL(FF8DH)	P1DL.7	P1DL.6	P1DL.5	P1DL.4	P1DL.3	P1DL.2	P1DL.1	P1DL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PxDH.y x = 0,2, y = 0-7	Port output high ability to reduce mode selection. 0: pin output mode is normal and high level. 1: pin output mode reduces high level.
7-0	P1DL.y y = 0-7	Port output low ability to reduce mode selection. 0: pin output mode is normal and low level. 1: pin output mode weakens the low level.

Application description: the driving capability equivalent to the output of the output is equivalent to that of the IO port, which can be used for the IIC communication port and save the external pull-resistance.
After the output is low, the driving capacity is equivalent to a 1K resistor connected with the IO port output, which can be used for some LED lights to drive the circuit and save the current resistance.
Table 7.24 Port input pull mode selection registers

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PHM(FF8EH)	P0PH.7	P0PH.6	P0PH.5	P0PH.4	P0PH.3	P0PH.2	P0PH.1	P0PH.0
P2PHM (FF8FH)	P2PH.7	P2PH.6	P2PH.5	P2PH.4	P2PH.3	P2PH.2	P2PH.1	P2PH.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

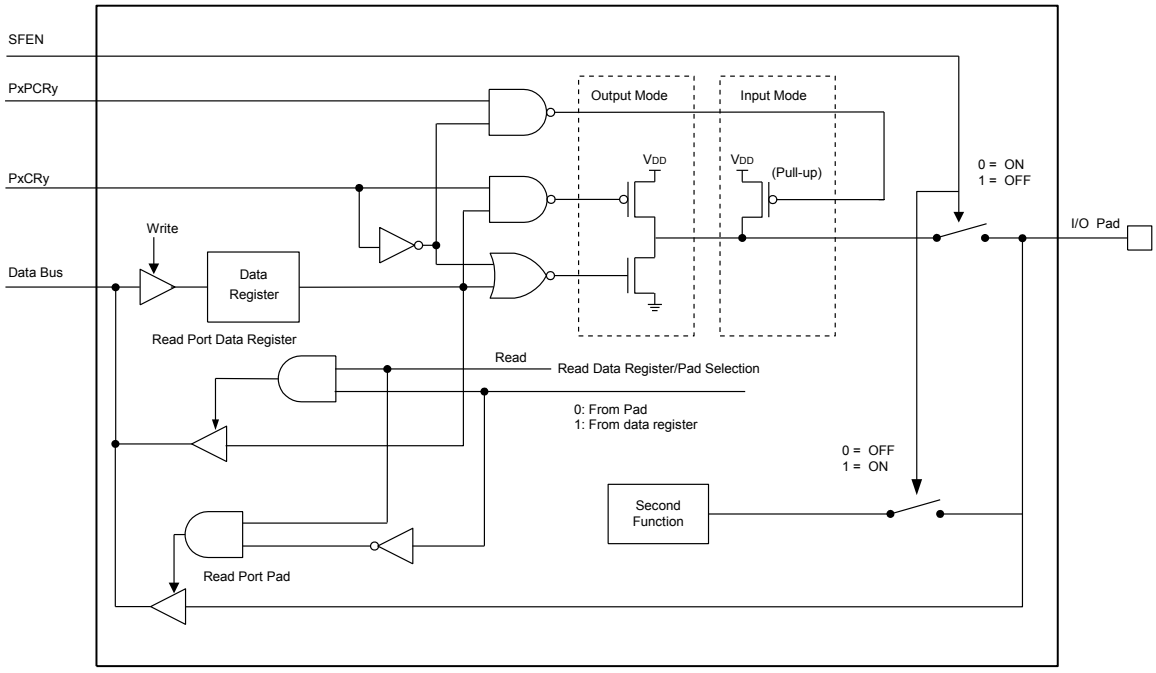
Bit Number	Bit Mnemonic	Description
7-0	PxPH.y x = 0,2	Port input pull mode selection 0: pin the pin into the normal mode. 1: input the pin input mode, The control bits only to a port on the corresponding effective after pulling resistance can, pull-up resistors value, depends on the input level, if the input is high level, pull-up resistors for normal pull-up resistor (30 k) + weak drive pull-up resistor (1 m), if The input level is low level and the pull-up resistance is weakly pull-up resistor (1M)

Application description: the pull-resistance switching mode on the port can be used for key input applications, saving the external pull of 1M resistance, while the high power is more capable of pulling power at ordinary times, which can overcome the external.
Changes in the environment, such as humidity caused by leakage of the key caused by incorrect press.
Table 7.25 Port data source selection.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0INM(FFFAH)	P0INM.7	P0INM.6	P0INM.5	P0INM.4	P0INM.3	P0INM.2	P0INM.1	P0INM.0
P2INM(FFFBH)	P2INM.7	P2INM.6	P2INM.5	P2INM.4	P2INM.3	P2INM.2	P2INM.1	P2INM.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PxINM.y x = 0,2	Port data source selection. 0：Output state，read port Registers，return port date registers value 1：Output state，read port Registers，return port level

7.6.3 Port Diagram



Note:
1) The input source of reading input port operation is from input pin directly.
2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly. The read Instruction distinguishes which path is selected.
3) The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.
4) The destination of writing Input / Output port operation is the data register.

7.6.4 Port Share

The 47 bi-directional I/O ports can also share second or third special function. But the share priority should obey the Outer Most Inner Lest rule:
The out most pin function in Pin Configuration has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin , even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.
When port share function is enabled, the user can modify PxCR, PxPCR(x=0~9), but these operations will have no effect on the port status until the second function was disabled.
When port share function is enabled, any read or write operation to port will only affect the data register while the port pin keeps unchanged until all the share functions are disabled.

PORT0：
- TXD3（P0.1）：EUART3 data output
- RXD3（P0.2）：EUART3 data input
- VIN (P0.3)：external voltage input
- INT40~INT43(P0.0-P0.3)：External interrupt input

Table 7.26 PORT0 Share Table

Pin No	Priority	Function	Enable bit
22	1	TXD3	Write SBUF3 Registers
	2	INT41	Without Priority1, the IO input function is still valid as the input port.
	3	P0.1	Above condition is not met
21	1	RXD3	Set up the SCON3 Registers REN3 bit1（Automatic upper）
	2	INT42	Without Priority1, the IO input function is still valid as the input port.
	3	P0.2	Above condition is not met
20	1	VIN	Code option
	2	INT43	Without Priority1, the IO input function is still valid as the input port.
	3	P0.3	Above condition is not met

PORT1：
- RSTB(P1.0) ：RESET pin
- QF(P1.3)：reactive energy pulse output
- PF(P1.4)：active energy pulse output
- CALOUT2(P1.4)：RTC Pulse output

Table 7.27 PORT1 Share Table

Pin No	Priority	Function	Enable bit
18	1	RSTB	Code option
	2	P1.0	Above condition is not met
64	1	QF	EMUCFG1Registers的QFEN=1
	2	P1.3	Above condition is not met
63	1	CALOUT2	RTCCONRegistersOUTEN[1:0]=11
	2	PF	EMUCFG1Registers的PFEN=1
	3	P1.4	Above condition is not met

PORT2：
- AN4（P2.2）：ADC input channel 4
- INT44（P2.2）：External interrupt input
- RXD0（P2.6）：EUART0 data input
- TXD0（P2.7）：EUART0 data output

Table 7.28 PORT2 Share Table

Pin No	Priority	Function	Enable bit
62	1	AN4	ADCHRegisters CH4 bits and ADCONRegisters ADON bits are 1，and SCH[3:0] = 0100
	2	INT44	Without Priority1, the IO input Function is still valid as the input port.
	3	P2.2	Above condition is not met
61	1	RXD0	Set up the SCONRegisters REN bits are 1（Automatic）
	2	P2.6	Above condition is not met
60	1	TXD0	Write SBUF Registers
	2	P2.7	Above condition is not met

PORT3：
- RXD1（P3.0）：EUART1 data input
- TXD1（P3.1）：EUART1data output

Table 7.29 PORT3 Share Table

Pin No	Priority	Function	Enable bit
91	1	RXD1	Set up the SCON1Registers REN1 bit are1（Automatic）
	2	P3.0	Above condition is not met
90	1	TXD1	Write SBUF1Registers
	2	P3.1	Above condition is not met

PORT4：
-COM1(SEG40)(P4.4): LCD COM or SEG port
-COM2(SEG41)(P4.5)：LCD COM or SEG port
-COM3(SEG42)(P4.6)：LCD COM or SEG port
-COM4(SEG43)(P4.7)：LCD COM or SEG port
Table 7.30 PORT4 Share Table

Pin No	Priority	Function	Enable bit
79	1	COM1(SEG40)	P4SS P4S4=1 and LCDCONRegisters LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P4.4	Above condition is not met
78	1	COM2(SEG39)	P4SS P4S5=1 and LCDCONRegisters LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P4.5	Above condition is not met
77	1	COM3(SEG38)	P4SS P4S6=1 and LCDCONRegisters LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	1	P4.6	Above condition is not met
76	1	COM4(SEG37)	P4SS P4S7=1 and LCDCONRegisters LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P4.7	Above condition is not met

PORT5：
-COM5(SEG1)(P5.0): LCD COM or SEG port
-COM6(SEG2)(P5.1)：LCD COMor SEG port
-COM7(SEG3)(P5.2)：LCD COMor SEG port
-COM8(SEG4)(P5.3)：LCD COMor SEG port
-SEG5-SEG8(P5.4-P5.7)：SEG port
Table 7.31 PORT5 Share Table

Pin No	Priority	Function	Enable bit
50	1	COM5(SEG1)	P5SS P5S0=1 and LCDCON Registers LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P5.0	Above condition is not met
49	1	COM6(SEG2)	P5SS P5S1=1 and LCDCON Registers LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P5.1	Above condition is not met
48	1	COM7(SEG3)	P5SS P5S2=1 and LCDCON Registers LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P5.2	Above condition is not met
47	1	COM8(SEG4)	P5SS P5S3=1 and LCDCON Registers LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P5.3	Above condition is not met
46	1	SEG5	P5SS P5S4=1 and LCDCON Registers LCDON=1

	2	P5.4	Above condition is not met
45	1	SEG6	P5SS P5S5=1 and LCDCON Registers LCDON=1
	2	P5.5	Above condition is not met
44	1	SEG7	P5SS P5S6=1 and LCDCON Registers LCDON=1
	1	P5.6	Above condition is not met
43	1	SEG8	P5SS P5S7=1 and LCDCON Registers LCDON=1
	2	P5.7	Above condition is not met

PORT6：
-SEG10-SEG16(P6.0-P6.7): LCD SEG□
Table 7.32 PORT6 Share Table

Pin No	Priority	Function	Enable bit
42-36	1	SEG10-SEG16	P6SS P6SX(X=0-7)=1 and LCDCON Registers LCDON=1
	2	P6.0-P6.7	Above condition is not met

PORT7：
-SEG17-SEG18/SEG22(P7.1/P7.1/P7.5): LCD SEG□
Table 7.33 PORT7 Share Table

Pin No	Priority	Function	Enable bit
35-33	1	SEG17-SEG24	P7SS P7SX(X=0-7)=1 and LCDCON Registers LCDON=1
	2	P7.0-P7.7	Above condition is not met

PORT8：
-SEG31-SEG32(P8.6-P8.7): LCD SEG□
Table 7.34 PORT8 Share Table

Pin No	Priority	Function	Enable bit
32-31	1	SEG31-SEG32	P7SS P8SX(X=0-7)=1 and LCDCON Registers LCDON=1
	2	P8.6-P8.7	Above condition is not met

PORT9：

-COM8(SEG33)-COM1(SEG40)(P9.0-P9.7): LCD COM port or SEG port

Table 7.35 PORT9 Share Table

Pin No	Priority	Function	Enable bit
43-36	1	-COM8(SEG33)-COM1(SEG40)(P9.0-P9.7)	P9SS P9SX(X=0-7)=1 and LCDCONRegisters LCDON=1，As COM or SEG is chosen by DUTY[3:0].
	2	P9.0-P9.7	Above condition is not met

7.7 TIMER

7.7.1 Features

The G80F975A has three independent 16-bit timers, Timer 0, Timer 1 and Timer 2.
Timer0 is compatible to traditional 8051.
Timer1is compatible to traditional 8051.
Timer 0/1 clock source selection
Timer 0/1 clock source divided by

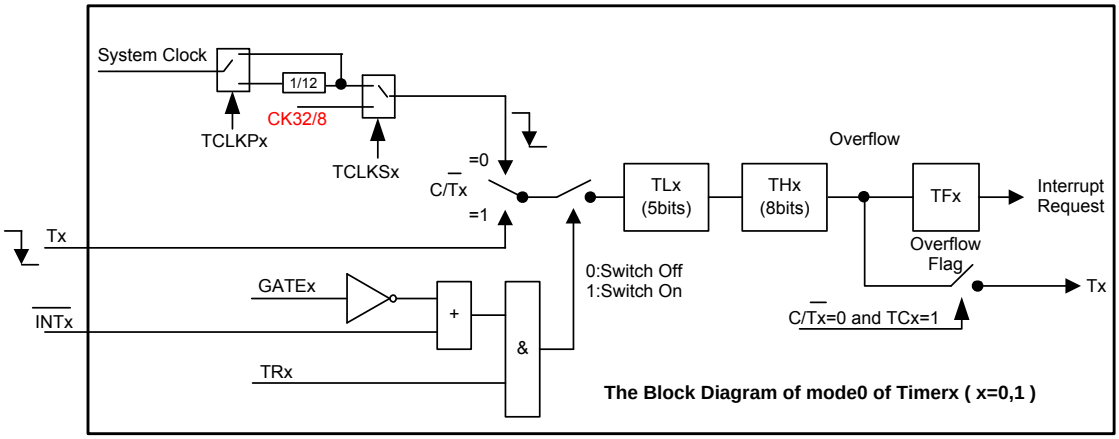
7.7.2 Timer0/1

Each regular two data registers (THx, and TLx acts as (for x = 0, 1)) can be used as a 16-bit register access. They are controlled by the registers TCON and TMOD. The ET0 of IEN0 register and ET1 position 1 allows the Timer 0 and Timer 1 interrupt. (Refer to the interrupt section).
Timer x mode（x = 0, 1）
Through the counter/timer mode Registers（TMOD）The way to choose bits Mx1-Mx0，Select the timer work mode.
Mode 0：13 bit counters/timers.

Timer 'x 13 counter / timers in Mode 0. THx register store 13-bit counter / timer 8 and TLx is stored 5 (TLx.4-TLx.0). Of TLx three (TLx.7-TLx.5) is uncertain, and should be ignored when read. When the 13-bit timer register increments, overflow, the system set up timer overflow flag TFx. If the timer x interrupt is enabled, will generate an interrupt. TCLKSx selects the counter / timer clock source.

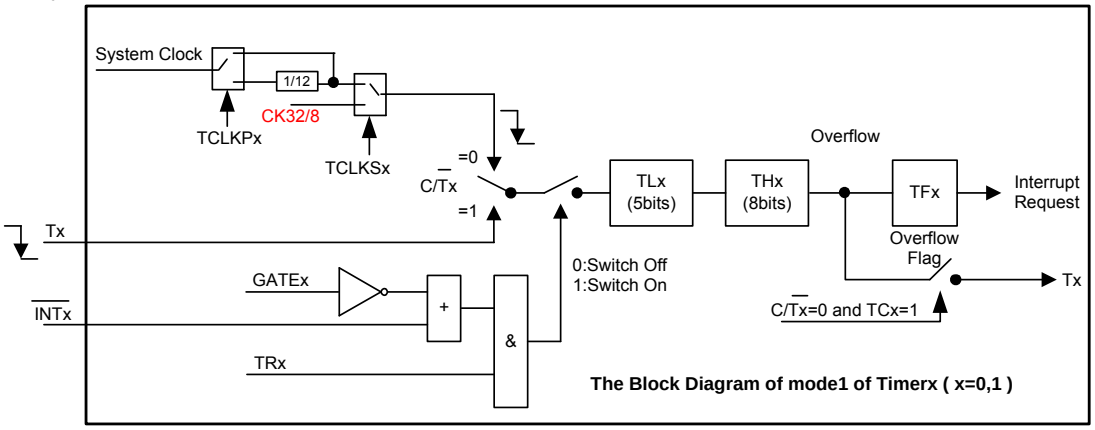
If the TCLKSx = 1, select CK32 is the clock source. If the TCLKSx = 0，select the system clock timer x is the clock source.

C/$\overline{Tx}$ position selection counter/timer working mode. If the C/$\overline{Tx}$= 1，Select to work the counter，Timer x input pins (Tx) level from high to low transition, so that the timer x data register plus 1.If the C/$\overline{Tx}$= 0，select timer x is the clock source.如果C/$\overline{Tx}$= 0，Choose to work the timer.
When the GATEx = 0, or GATEx = 1 and the input signal INTx effective TRx is set to open the timer. GATEx set to 1 allows the timer to INTx by the external input signal, control, ease of measurement INTx positive pulse width. TRx position not to force a reset timer, which means that if TRx is set, the timer register will start counting the last the TRx clear the value of 0:00. Therefore, before enabling the timer, set the initial value of the timer register.
The register TCON1 TCLKSx (x = 0,1) select the system clock or CK32 as timer x (x = 0,1) of the clock source can be configured as a timer application.
Configurable in TCLKPx (x = 0, 1) select the system clock or system clock 1/12 as the timer x (x = 0, 1) the clock source register TCON1.
For TC0 when the timer application, configuration the register TCON1 in / 1 so that the timer 0/1 overflow T0/T1 pin automatically flip. If TC0 / 1 is set to 1, the T0/T1 pin is automatically set as an output.

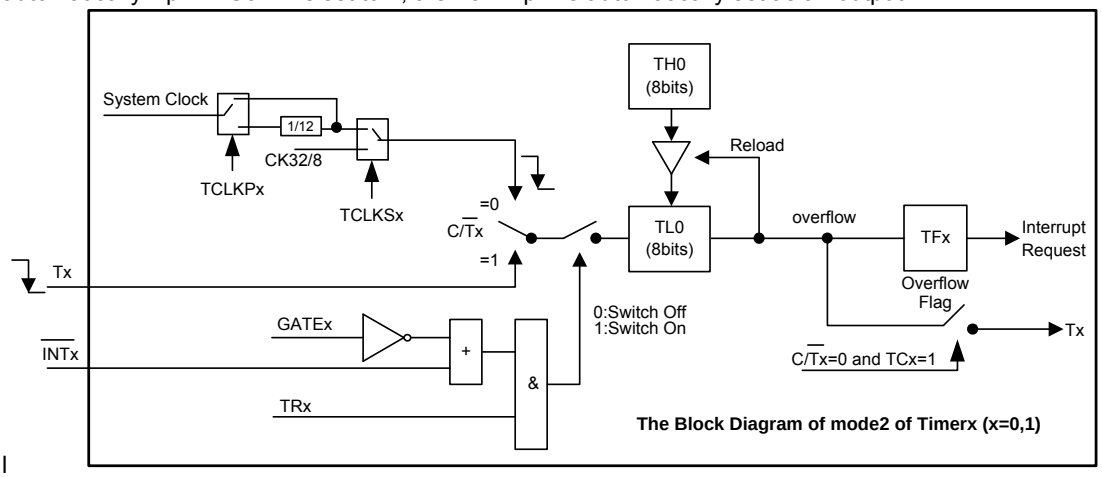


The Block Diagram of mode0 of Timerx (x=0,1)

Mode 1: 16-bit counter / timer
In addition to the 16-bit timer / counter, a run and the way of the way consistent. Open and configure the counter / timer also as a way to 0.



Mode 2: 8-bit auto-reload counter / timer
Mode 2, Timer x is 8-bit auto-reload counter / timer. TLx store the count value of THx, store the reload value. When in TLx counter overflows to 0x00, set from the timer overflow flag TFx, the values of the registers THx reload register TLx. If the timer interrupt is enabled, when TFx set will generate an interrupt. The reload value in THx will not change. Allows the timer to the correct count before the start, TLx must be initialized to the desired value.
In addition to auto-reload function, mode 2 counter / timer enable and configuration mode 1 and 0 is the same.
When the timer application that can be configured the register TCON1 TCLKSx (x = 0, 1) bits select the system clock or 32.768kHz/8 timer x (x = 0, 1) the clock source.
Configurable in TCLKPx (x = 0, 1) select the system clock or system clock 1/12 as the timer x (x = 0, 1) the clock source register TCON1.
For TC0 when the timer application, configuration the register TCON1 in / 1 so that the timer 0/1 overflow T0/T1 pin automatically flip. If TC0 / 1 is set to 1, the T0/T1 pin is automatically set as an output.



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mode 3：Two 8-bit counters/timers (limited to timer 0)

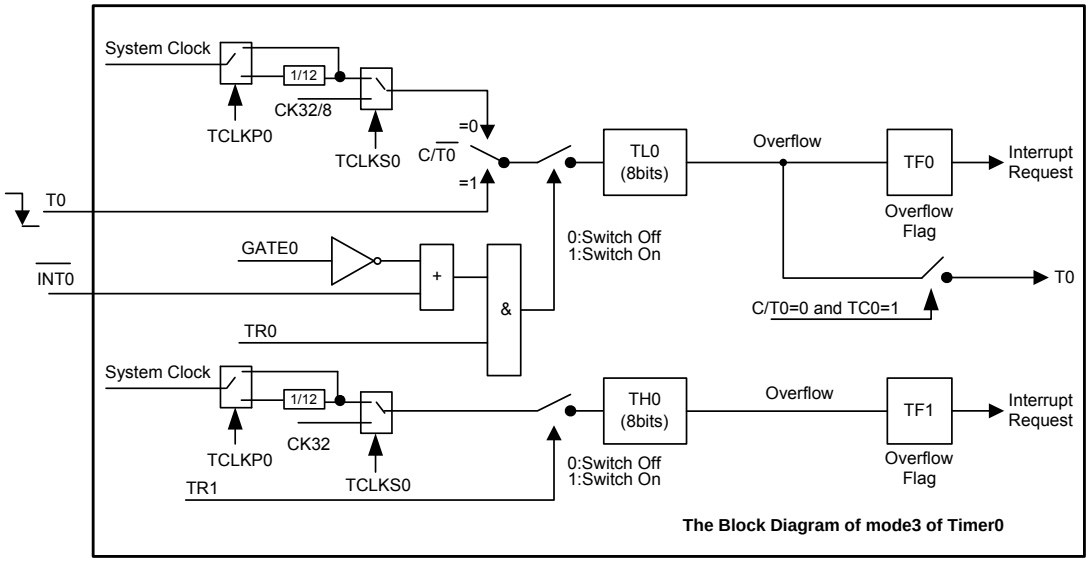
In Mode 3, Timer 0 is used as two independent 8-bit counter / timer, TL0 and TH0 control.The TL0 use the Timer 0 control (in TCON) and status (in TMOD) bits: TR0, C/T0GATE0 and TF0. The TL0 use the system or CK32 or an external,input signal as a clock source.

TH0 can only be used as the timer clock source from the system clock. The TH0 by Timer 1 control bit TR1 control is enabled, the overflow Timer 1 overflow flag TF1 set, Control Timer 1 interrupt.

Timer 0 in Mode 3, Timer 1 can operate in modes 0, 1 or 2, but not at 1 TF1 flag and generate an interrupt. TH1 and TL1 can only be used as a timer function, the clock source from the system clock, bit invalid GATE1. T1 input pin pull-up resistor is not valid. Timer 1 enabled or not, because the control of TR1 Timer 0 occupied. Timer is enabled, the one in the way 0, 1 or 2:00 in Mode 3 is turned off.

Register TCON1 the TCLKS0 select the system clock or 32.768kHz/8 as the timer clock source can be configured as a timer application.Can be configured to register TCON1 the TCLKP0 select the system clock or system clock 1/12 as the clock source of timer 0.

When the timer application, configuration the register TCON1 in TC0 overflow of Timer 0 T0 pin automatically flip. If TC0 is set to 1, the T0 pin is automatically set as an output.



The Block Diagram of mode3 of Timer0

Registers

Table 7.36 Timer / Counter x control register (x = 0,1)

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7, 5	TFx x = 0, 1	Timer x overflow flag 0: Timer x overflow, can be cleared by software. 1: Timer x overflow is set by hardware; by software set to 1 will cause the timer interrupt
6, 4	TRx x = 0, 1	Timer x to start, stop control bit 0: stop the timer x 1: Start the timer x

Table 7.37 Timer / counter MODE register (x = 0,1)

89H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMOD	GATE1	C/$\overline{T1}$	M11	M10	GATE0	C/$\overline{T0}$	M01	M00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7, 3	GATEx x = 0, 1	Timer x gate position. 0: TRx set 1, timer x is allowed. 1: only INTx(--) is allowed during the high level of TRx 1 and timer x.
6, 2	C/$\overline{Tx}$ x = 0, 1	Select the timer/counter mode. 0: timer mode. 1. Counter mode
5-4 1-0	Mx[1:0] x = 0, 1	Timer x timer mode selection. 00: method 0,13 digit counting counter/timer, ignoring the 7th to 5th position of TLx. 01: method 1,16 bits up counter/timer. 10: mode 2,8 bit automatic overload counting counter/timer. 11: mode 3 (for timer 0 only), two 8-bit counting timers.

Table 7.38 Timer / counter data register (x = 0,1)

8AH-8DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL0 (8AH)	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0
TH0 (8CH)	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0
TL1 (8BH)	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0
TH1 (8DH)	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description

7-0	TLx.y, THx.y x = 0-1, y = 0-7	Timer x low and high byte counter.

Table 7.39 Timer / counter control register (x = 0,1)

8FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON1	-	TCLKS1	TCLKS0	-	TCLKP1	TCLKP0	TC1	TC0
R/W	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-5	TCLKSx x = 0,1	The timer x clock source control bit. 0: system clock is the clock source of timer x. 1: select CK32 as the clock source of timer x.
3-2	TCLKPx x = 0,1	The timer x clock source prefrequency control bit. 0: select 1/12 of the system clock as the clock source of timer x. 1: select the system clock as the clock source of timer x.
1-0	TCx x = 0,1	Compare the output FunctionEnable bit. 0: the timer x is forbidden to compare output Function. 1: allow timer x to compare output Function.

7.7.3 Timer2

The Timer 2 in the G80F975A is the standard C52 Timer 2.It is implemented as a 16-bit register accessed as two cascaded Data Registers: TH2 and TL2. It is controlled by the register TCON2 and TMOD2. The Timer 2 interrupt can be enabled by setting ET2 bit in IEN0 register (See Interrupt section).
For Timer2 operation, C/T2 selects system clock (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows Timer 2/Counter 2 Data Register to increment by the selected input.
TCLKP2 in T2MOD selects system clock or 1/12 system clock as the Timer 2 clock source.

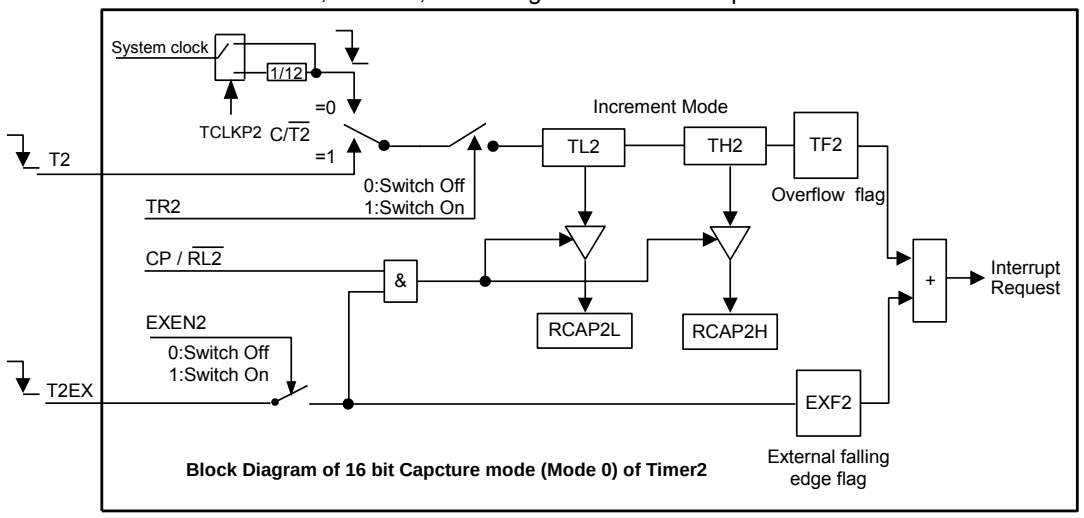
Timer 2 Modes

Timer 2 has three kinds of work: Capture / Reload with increment or decrement the counter of the auto-reload mode and programmable clock output. CP/RL2 combination of selection of these ways.
Timer 2 Modes select

C/$\overline{T2}$	T2OE	DCEN	TR2	CP/RL2	方式	
X	0	X	1	1	0	16 bit capture
X	0	0	1	0	1	16 bit auto-reload timer
X	0	1	1	0		
0	1	X	1	X	2	Programmable clock-output only
1	1	X	1	X	X	Not suggest to use this mode
X	X	X	0	X	X	Timer2 stop, the T2EX path still enable

Mode 0: 16 bit Capture

In the capture mode, two options are selected by bit EXEN2 in T2CON.
If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which will set TF2 on overflow to generate an interrupt if IET2 is enabled.
If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L respectively, In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can also generate an interrupt if IET2 is enabled.

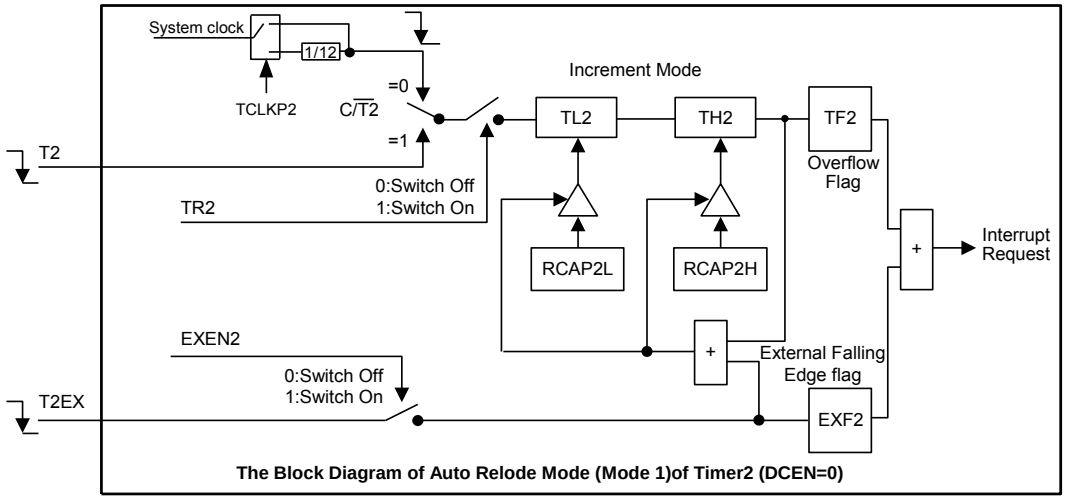


Block Diagram of 16 bit Capcture mode (Mode 0) of Timer2

Mode 1: 16 bit auto-reload timer

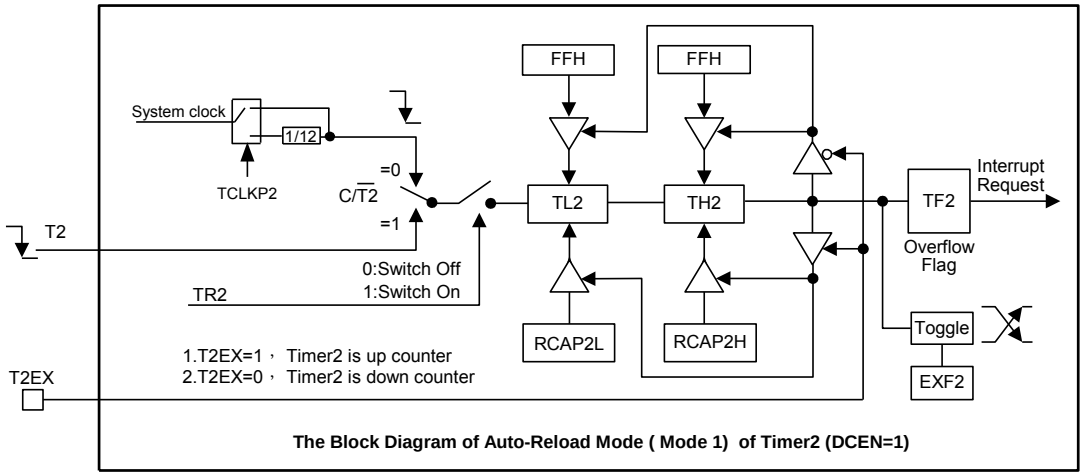
Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by DCEN (Down Counter Enable) bit in T2MOD. Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

When DCEN=0, two options are selected by bit EXEN2 in T2CON.
If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software.
If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.



The Block Diagram of Auto Relode Mode (Mode 1)of Timer2 (DCEN=0)

Setting the DCEN bit enables Timer 2 to count up or down. When DCEN = 1, the T2EX pin controls the direction of the count, and EXEN2's control is invalid.
A logical "1" at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.
A logical "0" at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.
The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.



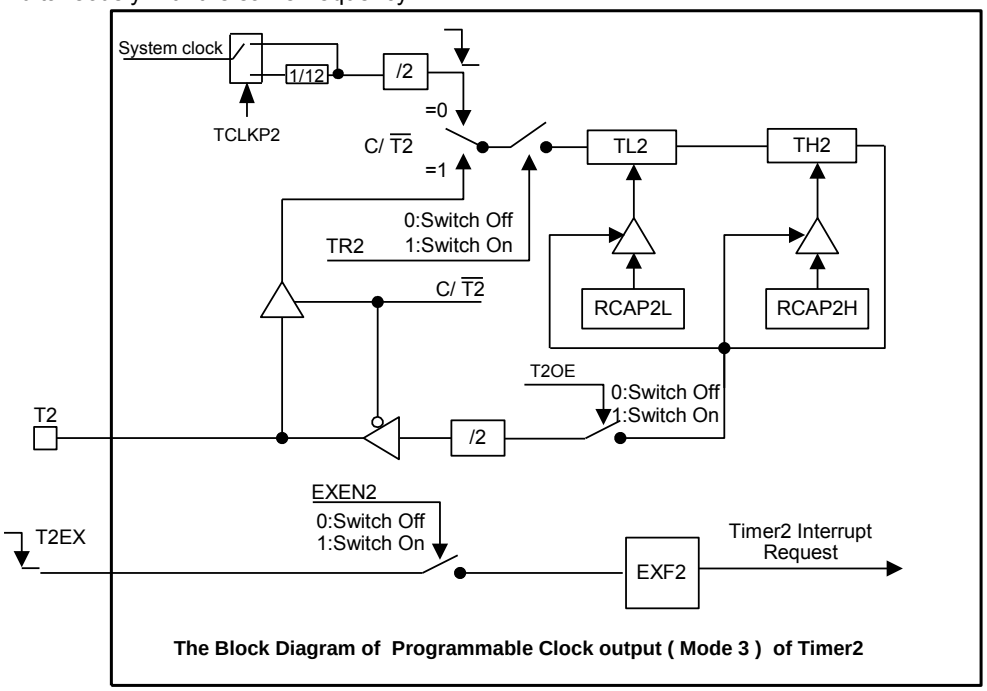
The Block Diagram of Auto-Reload Mode (Mode 1) of Timer2 (DCEN=1)

Mode 3: Programmable Clock output

In this mode the clock-out frequency depends on the system clock and the reload value of Timer 2 Capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock Out Frequency} = \frac{1}{2\times 2} \times \frac{\text{System Clock}}{65536 - [\text{RCAP2H,RCAP2L}]}$$

Timer 2 overflow will not generate an interrupt, so it is possible to use Timer 2 as a baud-rate generator and a clock output simultaneously with the same frequency.



The Block Diagram of Programmable Clock output (Mode 3) of Timer2

Note:
(1) TF2 and EXF2 both can generate an interrupt and share the same interrupt vector address.
(2) TF2 and EXF2 can be set to '1' in any conditions, and they can be cleared only by software or hardware reset.
(3) When EA = 1 and ET2 = 1, it generates the Timer 2 interrupt by setting TF2&EXF2=1.
(4) 4&5 bits in T2CON can't be writtern other than '0', otherwise T2 may not work.

Registers

Table 7.40 Timer 2 Control register

C8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2	-	-	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	TF2	Timer2 overflow flag bit 0 = No overflow (Must be cleared by software) 1 = Overflow (Set by hardware if RCLK = 0 & TCLK = 0)
6	EXF2	External event input (falling edge) from T2EX pin detected flag bit. 0 = No external event input (Must be cleared by software) 1 = Detected external event input (Set by hardware if EXEN2 = 1)
3	EXEN2	External event input (falling edge) from T2EX pin used as Reload/Capture trigger enable/disable control bit 0 = Ignore events on T2EX pin for Timer 2 operation 1 = Cause a capture or reload when a negative edge on T2EX pin is detected, when Timer 2 is not used to clock the EUART (T2EX always has a pull up resistor)
2	TR2	Timer2 start/stop control bit 0 = Stop Timer 2 1 = Start Timer 2
1	C/$\overline{T2}$	Timer 2 Timer / Counter mode selected bit 0 = Timer Mode, T2 pin is used as I/O port 1 = Counter Mode, the internal pull-up resister is turned on
0	CP/$\overline{RL2}$	Capture/Reload mode selected bit 0 = 16 bits timer/counter with reload function 1 = 16 bits timer/counter with capture function

Table 7.41 Timer 2 Mode Control register

C9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	TCLKP2	-	-	-	-	-	T2OE	DCEN
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7	TCLKP2	Frequency devision select: 0: Select 1/12 system clock as Timer 2 clock source. 1: Select system clock as Timer 2 clock source.
1	T2OE	Timer 2 Output Enable bit 0 = Set P3.2/T2 as clock input or I/O port. 1 = Set P3.2/T2 as clock output (Baud-Rate generator mode)
0	DCEN	Down Counter Enable bit 0 = Disable Timer 2 as up/down counter, timer 2 is an up counter. 1 = Enable Timer 2 as up/down counter.

Table 7.42 Timer 2 Reload/Capture & Data Registers

CAH-CDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCAP2L (CAH)	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H (CBH)	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2 (CCH)	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2 (CDH)	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	RCAP2L.x	Timer 2 Reload/ Capturer Data, x=0~7
	RCAP2H.x	
7-0	TL2.x	Timer 2 Low & High byte counter, x=0~7
	TH2.x	

7.8 Interrupt

7.8.1 Features

11 interrupt sources
4 interrupt priority levels
Program Over Range interrupt

G80F975A 11 interrupt sources: 1 External interrupt, three timer interrupts (timer 0/1/2), 3 EUART interrupts, ADC interrupt, The RTC interrupt , LPD interrupt and EMU interrupt.

7.8.2 Interrupt Enable control

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global interrupt enable bit, EA, which can enable/disable all interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that the corresponding interrupts are disabled.

Table 7.43 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADTP	ET2	ES0	ET1	E7816	ET0	EX4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	EA	All Interrupt Enable bit 0: Disable all interrupts 1: Enable all interrupts
6	EADTP	ADC Interrupt Enable bit 0: Disable ADC interrupt 1: Enable ADC interrupt
5	ET2	Timer 2 Interrupt Enable bit 0: Disable Timer 2 interrupt 1: Enable Timer 2 interrupt
4	ES0	EUART0 Interrupt Enable bit 0: Disable EUART0 interrupt 1: Enable EUART0 interrupt
3	ET1	Timer 1 Interrupt Enable bit 0: Disable Timer 1 interrupt 1: Enable Timer 1 interrupt
2	E7816	7816 Interrupt Enable bit 0：Disable SPI interrupt 1：Enable SPI interrupt
1	ET0	Timer 0 Interrupt Enable bit 0: Disable Timer 0 interrupt 1: Enable Timer 0 interrupt
0	EX4	Interrupt 4 Enable bit 0: Disable External Interrupt 4 1: Enable External Interrupt 4

Table 7.44 Primary Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	ES3	-	ELPD	-	-	ES1	ERTC	EEMU
R/W	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	-	0	-	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	ES3	EUART3 Interrupt Enable bit 0: Disable EUART3 interrupt 1: Enable EUART3 interrupt
5	ELPD	LPD interrupt Enable bit 0：Disable LPD interrupt 1：Enable LPD interrupt
2	ES1	EUART1 interrupt Enable bit 0：Disable EUART1 interrupt 1：Enable EUART1 interrupt
1	ERTC	RTC interrupt Enable bit 0：Disable RTC interrupt 1：Enable RTC interrupt
0	EEMU	Energy Metering Interrupt Enable bit 0：Disable EMU interrupt 1：Enable EMU interrupt

Table 7.45 External interrupt channel allows Registers

AAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IENX	-	-	-	EXS44	EXS43	EXS42	EXS41	-
R/W	-	-	-	R/W	R/W	R/W	R/W	-
Reset Value（POR/WDT/LVR/PIN）	-	-	-	0	0	0	0	-

Bit Number	Bit Mnemonic	Description
4-1	EXS4x（x = 1-4）	External interrupt 4 choice Registers （x = 1-4） 0：Disable External interrupt 4x 1：Enable External interrupt 4x

7.8.3 Interrupt Flag

Each interrupt source has its own interrupt flag, when an interrupt is generated, the hardware will be set from the corresponding flag Individual interrupt flag bits are listed in the interrupt summary table.

External interrupt interrupted INT4, IXF1Registers IF4x symbol of a (x = 1 to 4) 1, because INT4x sharing an interrupt vector address, so mark a software requires the user to remove.

However, if INT4 is triggered by the level, the flag bit cannot be cleared by the user's software, only the signal level directly controlled by INT4x interrupt source pin.

0/1 of the timer counter overflow, the TCON register TFx (for x = 0, 1) interrupt flag, resulting in the Timer 0/1 interrupt the CPU after the interrupt flag is hardware automatically cleared.

T2CON register TF2 or EXF2 flag, generate timer interrupt, the CPU after the interrupt, the flag can not be hardware automatically cleared. In fact, the interrupt service routine must decide whether an interrupt is generated by the TF2 or EXF2 flag must be cleared by software.

SCON register sign of RI or TI is set to 1, resulting in EUARTx (x = 0，1，2，3) interrupt the CPU after the interrupt flag is not by hardware automatically cleared. In fact, the interrupt service routine must determine whether the received interrupt or an interrupt flag must be cleared by software.

ADCON register ADCIF flag 1:00, resulting in the ADC interrupt. If the interrupt is generated, the ADDH / ADDL the, result of the conversion is valid. Continuous comparison function of the ADC module is turned on if the result is greater than the comparison value, conversion, if the conversion result is less than the comparison value, the ADCIF flag 0;, ADCIF flag ADCIF interrupt flag must be performed by software cleared.

SPSTA Registers SPIF or MODF flag=1（SSDIS=0），resulting in SPI interrupt .These flags must be cleared by software.

RTCIF register IT0IF or DAYIF or HRIF or MINIF or SECIF or ALM1IF or ALM0IF flag=1, resulting in RTC interrupt. These flags must be cleared by software.

The LPDCON register LPDIF flag is set, LPD generate an interrupt. CPU in the response of the interrupt flag is hardware automatically clears.

Setting the corresponding EMUIF register after a energy metering period, then AND with the EMUIE register, if the result isn't zero, the EXF0 register EMUF flag, resulting in the EMU interrupt. The flag must be cleared by software

Table 7.46 External Interrupt Flag Register（x = 0，1）

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7, 5	TFx (x = 0, 1)	Timer x overflow flag 0: Timer x overflow, can be cleared by software. 1: Timer x overflow is set by hardware; by software set to 1 will cause the timer interrupt
6, 4	TRx (x = 0, 1)	Timer x to start, stop control bit 0: stop the timer x 1: Start the timer x

Table 7.47 External Interrupt 4 Control Registers

ABH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXCON1	-	-	IT4.5	IT4.4	IT4.3	IT4.2	IT4.1	IT4.0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/PIN）	-	-	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description

5-4	IT4 [5：4]	External Interrupt INT44，INT46 trigger mode 00 = Low Level trigger 01 = Trigger on falling edge 10 = Trigger on rising edge 11 = Trigger on both edge
3-2	IT4 [3：2]	External Interrupt INT41，INT43 trigger mode 00 = Low Level trigger 01 = Trigger on falling edge 10 = Trigger on rising edge 11 = Trigger on both edge
1-0	IT4 [1：0]	External Interrupt INT40，INT42 trigger mode 00 = Low Level trigger 01 = Trigger on falling edge 10 = Trigger on rising edge 11 = Trigger on both edge

Table 7.48 External Interrupt 4 Flag Register

E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF0	IF4.7	IF4.6	IF4.5	IF4.4	IF4.3	IF4.2	IF4.1	IF4.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （POR/WDT/LVR/PIN）	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	IF4x （x = 0-7）	External interrupt 4 request sign, IF4x must be cleared by software 0. 0：No interrupt request 1：Interrupt request

7.8.4 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in Interrupt Summary Table.

7.8.5 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. The interrupt priority service is described below:

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction cycle, an internal polling sequence determines which request is serviced.

Interrupt Priority Leve		
Priority bits		Interrupt Level Priority
IPHx	IPLx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.49 Interrupt priority control registers

B8H, BAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL0 (B8H)	-	PADCL	PT2L	PS0L	PT1L	P7816L	PT0L	PX4L
IPH0 (BAH)	-	PADCH	PT2H	PS0H	PT1H	P7816H	PT0H	PX4H
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

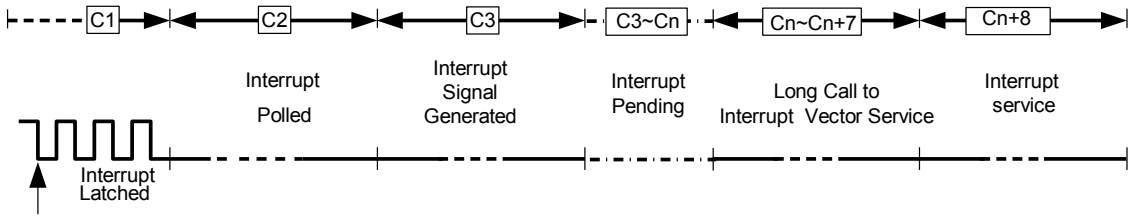
Reset Value(POR/WDT/LVR/ PIN)	-	0	0	0	0	0	0	0
B9H, BBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL1 (B9H)	PS3L	PTKL	PLPDL	PS2L	PSPIL	PS1L	PRTCL	PEMUL
IPH1 (BBH)	PS3H	PTKH	PLPDH	PS2H	PSPIH	PS1H	PRTCH	PEMUH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PxxxL/H	Corresponding interrupt source xxx's priority level select

7.8.6 Interrupt Handling

The interrupt flags are sampled and polled at the fetch cycle of each machine cycle. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:
An interrupt of equal or higher priority is already in progress.
2. The current cycle is not in the final cycle of the instruction in progress. This ensures that the instruction in progress is completed before vectoring to any service routine.
The instruction in progress is RETI. This ensures that if the instruction in progress is RETI then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.
Notes: Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between the these 2 instructions during the change of priority.

Note that if the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling cycle interrogates only the valid interrupt requests.
The polling cycle/LCALL sequence is illustrated below



Interrupt Response Timing
The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with corresponding address that depends on the source of the interrupt being vectored too, as shown in Interrupt Summary table.
Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt service. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt with this priority was still in progress. In this case, no interrupt of the same or lower priority level would be acknowledged.

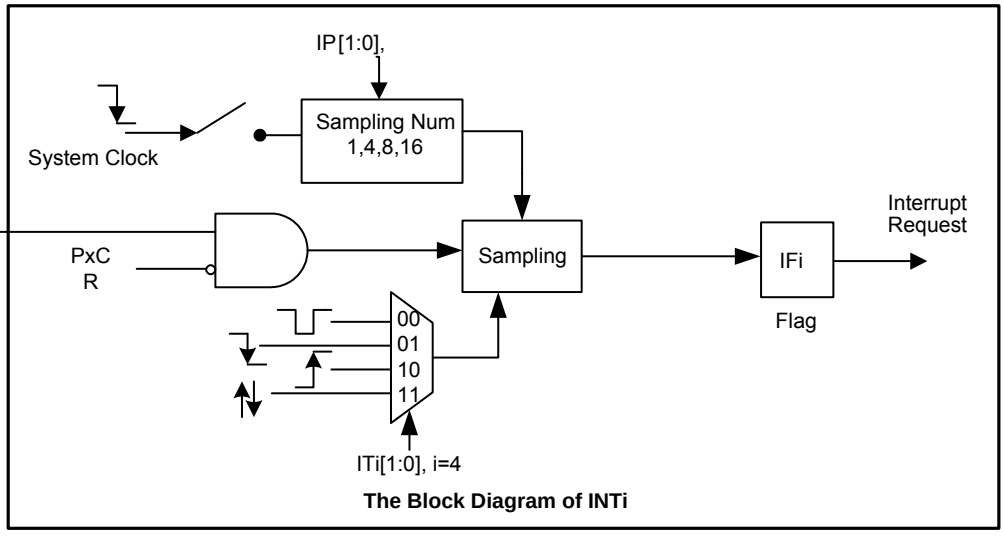
7.8.7 nterrupt Response Time

The SH79F642B has 4 external interrupt inputs. External interrupt 1-3 each has one vector address. External interrupt 0/1 can be programmed to be level-triggered or edge-triggered by clearing or setting bit IT1 or IT0 in register TCON and register EXF0. If ITn = 0(n=0~1), external interrupt 0/1 is triggered by a low level detected at the INT1 pin. If ITn =1(n=0~1), external interrupt 0/1 is edge triggered. In this mode if consecutive samples of the INT1 pin show a high level in one cycle and a low level in the next cycle, interrupt request flag in register EXF1 is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine cycle, an input high or low level should be held for at least one machine cycle to ensure proper sampling.

If the external interrupt is edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag is set. Notice that IE0-3 is automatically cleared by CPU when the service routine is called.
External interrupt2-3 operates in the similar ways except have different registers and have more selection of trigger.
If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag Iex (x=1,2,3) when the interrupt is level sensitive, it simply tracks the input pin level.
If an external interrupt is enabled when the SH79F642B is put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation. Refer to the Power management Section for details.

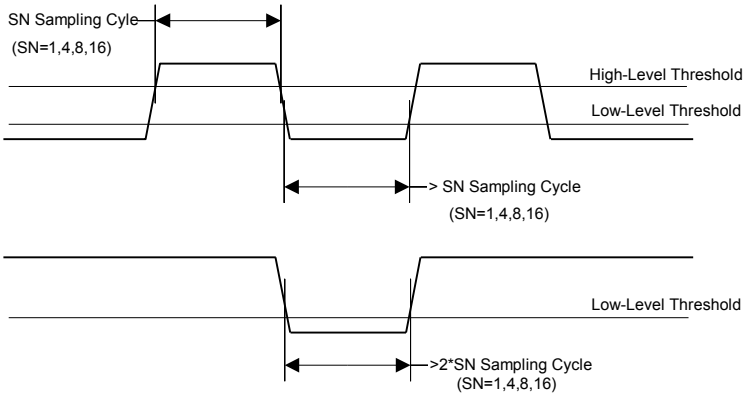
7.8.8 External Interrupt inputs

The G80F975A has 8 external interrupt inputs. The eight interrupt sources of external interrupt 4 share an interrupt vector address.
4 external interrupt can be set by EXF0Registers IT4 [1:0] is to select the level trigger or edge trigger.
When IT4[1:0]=00, the external interrupt int40-47 pins are triggered by low level;
When IT4[1:0]=01, the external interrupt int40-47 is triggered by the descending edge;
When IT4[1:0]=10, the external interrupt int40-47 is triggered by the rising edge;
When IT4[1:0]=11, the external interrupt int40-47 is triggered by the double edge.
If the external interrupt is rising along the trigger, a sampling period INT4x pins on continuous sampling for the low level, and the next cycle begins, continuous sampling of SN cycles for high level (SN for sampling frequency), interrupt request logo position 1, send out an interrupt request.
Since the external interrupt pin is sampled once per cycle, the input high or low level should maintain at least the SN cycle to ensure that it is properly sampled.
If the external interrupt is edge-triggered, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag is set.
If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine cycles. If the external interrupt is still asserted when the interrupt service routine is completed, another interrupt will be generated. It is not necessary to clear the interrupt flag Iex (x=1,2,3) when the interrupt is level sensitive, it simply tracks the input pin level.
f an external interrupt is enabled when the G80F975Ais put into Power down or Idle mode, the interrupt occurrence will cause the processor to wake up and resume operation. Refer to the Power management Section for details.



The Block Diagram of INTi

Notes: external interrupt 4 flag IF40-47must be cleared by software 0。



External Interrupt Detection

Table 7.50 External Interrupt port 4 mode Control Register 2

ACH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXCON2	I1PS1	I1PS0	IP.1	IP.0				
R/W	R/W	R/W	R/W	R/W				
Reset Value （POR/WDT/LVR/PIN）	0	0	0	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7-6	I1PS[1:0]	External interrupt INT4 sampling clock prefrequency ratio selection. 00：1/1 01：1/4 10：1/16 11：1/64
5-4	IP[1：0]	External interrupt port level sampling control. 00：Sampling 1 time, the logic level is valid. 01：For two consecutive samples, the same logic power is equally valid. 10：For three consecutive samples, the same logic power is equally valid. 11：For four consecutive samples, the same logic power is equally valid.

7.8.9 Interrupt Summary

Source	Vector Address	Enable bit	Flag bits	Polling Priority	C51
Reset	0000h	-	-	0 (Highest)	-
INT4	0003H	EX4+IENC	IF40-47	1	0
TIMER0	000BH	ET0	TF0	2	1
TIMER1	001BH	ET1	TF1	4	3
EUART0	0023H	ES	RI+TI	5	4
TIMER2	002BH	ET2	TF2+EXF2	6	5
ADC/TPS	0033H	EADTP	ADTPIF	7	6
EMU	003BH	EEMU+EMUIE	EMUIF	8	7
RTC	0043H	ERTC+RTCIE	RTCIF	9	8
EUART1	004BH	ES1	RI1+TI1	10	9
LPD1	0063H	ELPD13	LPD1IF	13	12
TK	006BH	ETK	TKF0	14	13
EUART3	0073H	ES3	RI3+TI3	15	14

8.Enhanced Function

8.1 LCD Driver

The LCD driver contains a controller, 4/6/8 common signal pads and 36 segment driver pads. Segment 1~40 and COM1~COM8 can also be used as I/O port, it is controlled by the P4SS、P5SS、P6SS、P7SS、P8SS、P9SS registers.

The 40 byte display data RAM is addressed at 2500H-2527H, which could be used as data memory if needed.

The G80F975A uses normal display topologies with contrast adjustment and which supports both 1/4duty-1/3 or 1/4 bias and 1/8duty-1/4bias. In addition, it supports FCM (Fast Charge Mode) to reduce power cost.

The LCD supply power VLCD equals to VOUT. or Powered by 3V LDO.

LCD driving voltage VLLCD is equal to VOUT LCD COM position adjustable.

During the Power on Reset or Pin Reset or LVR Reset or Watch-dog Reset, the LCD will be turned off.

When LCD is turned off, both common and segment will output low.

8.1.1 Resistance-type LCD model

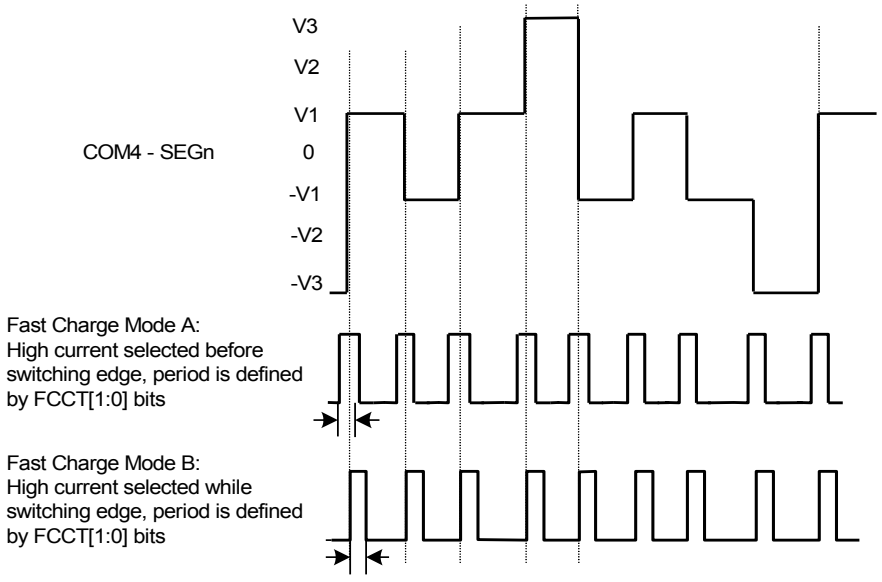
The traditional resistance-type LCD display modes have the following characteristics:

- Register by CONTR [2:0] in LCDCON control 8 contrast adjustment;
- 1/4 duty cycle when the frame rate of 64Hz;
- Support for fast charging mode (Fast Charge Mode) in order to reduce power consumption.

The from LCDCON2 Rregister MOD [2:0] bits control selectable LCD bias resistor (RLCD) for 60k or 900k. Select the 60k bias resistor can get a better display, but the current will be relatively large, not suitable for low power applications. The MOD [2:0] bits in LCDON2are set for 011 select 60k/900k bias resistor, although you can achieve low power consumption, but the LCD display will become worse.

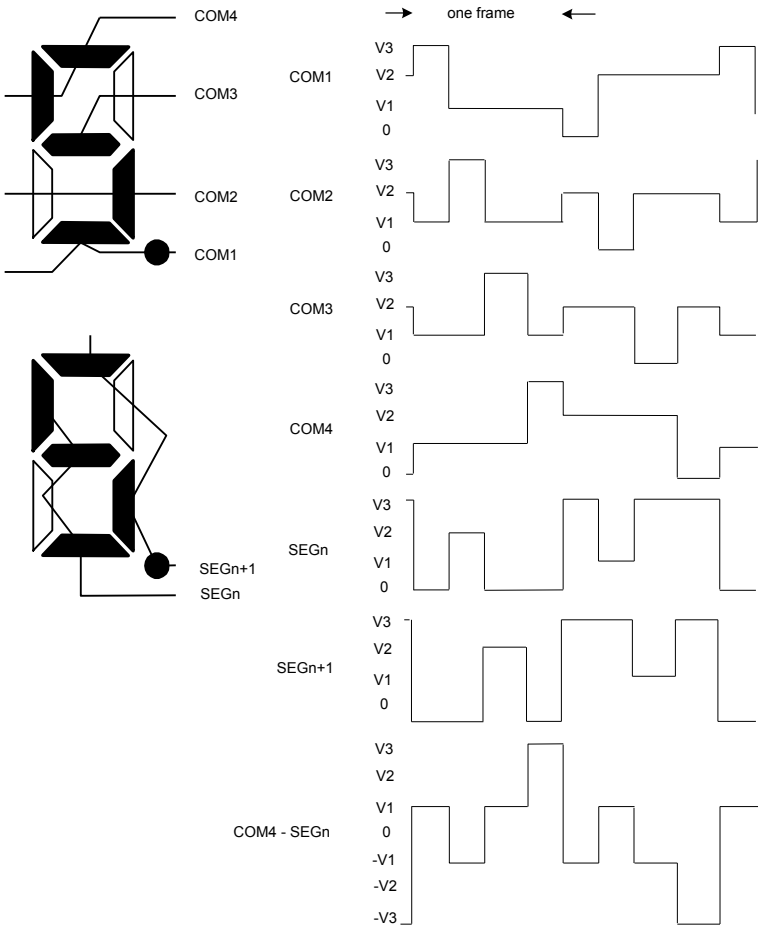
Therefore, MCU provides both low power and display the display mode: fast charge mode. Set the MOD [2:0] = 1xx can choose such a display, 60k bias resistor in the display data refresh time, provide greater drive current, selected during the data retention 1.5M bias resistor to provide a smaller drive current.

Fast charging display two charging modes: Mode A and Mode B byLCDCON2 register FCMOD bit to choose. From LCDCON2 register FCCTL [1:0] bits select the charging time LCD com cycle of 1/4, 1/8, 1/16 or 1/32.

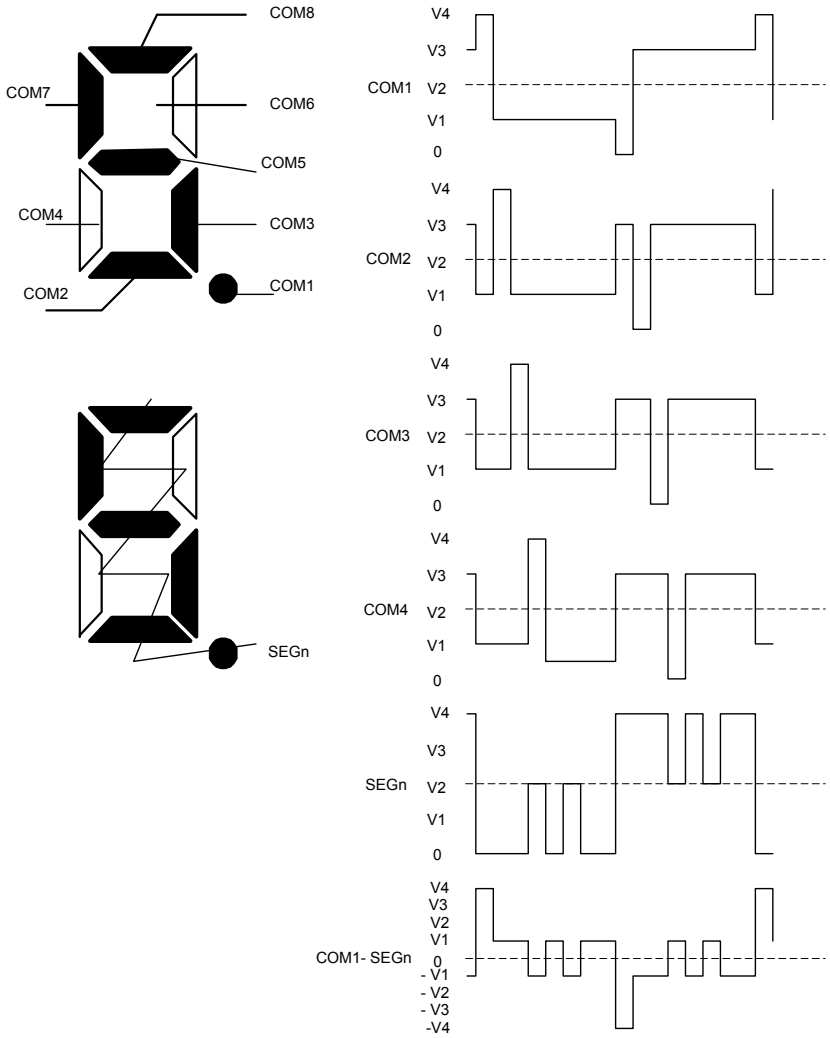


Fast Charge Mode Waveform

LCD waveform



LCD waveform (1/4duty, 1/3bias)



LCD waveform (1/8duty, 1/4bias)

8.1.2 Registers

Table 8.1 LCD Control Register

D1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON1	LCDON	DUTY2	DUTY1	DUTY0	BIAS	CONTR2	CONTR1	CONTR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	LCDON	LCD on/off control bit 0 = LCD display Off (default) 1 = LCD display On
6-4	DUTY[2:0]	LCD duty selector: 000: 1/4 duty, 1/3 bias recommended, P4.4-P4.7 is used as COM1-COM4 001: 1/4 duty, 1/3 bias recommended, P9.7-P9.4 is used as COM1-COM4 010: 1/6 duty, 1/3 bias recommended, P4.4-P4.7、 P5.0-P5.1 is used as COM1-COM6 011: 1/6 duty, 1/3 bias recommended, P9.7-P9.2 is used as COM1-COM6 100: 1/8 duty, 1/4 bias recommended, P4.4-P4.7、P5.0-P5.3is used as COM1-8 101: 1/8 duty, 1/4 bias recommended, P9.7-P9.0is used as COM1-8 other:=000
3	BIAS	BIAS selector: 0：1/3 bias 1：1/4 bias
2-0	CONTR[2:0]	LCD contrast control 000：VLCD = 0.600 VOUT 001：VLCD = 0.660 VOUT 010：VLCD = 0.720 VOUT 011：VLCD = 0.780 VOUT 100：VLCD = 0.840 VOUT 101：VLCD = 0.900 VOUT 110：VLCD = 0.960 VOUT 111：VLCD = 1.000 VOUT

Table 8.2 LCD Contrast Control Register

D2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON2	FCMOD	-	FCCTL1	FCCTL0	LCDLDOEN	MOD2	MOD1	MOD0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	FCMOD	Fast charge up mode control: 0: fast charge up mode A 1: fast charge up mode B
5-4	FCCTL[1:0]	Fast charge up time control : 00: 1/4 LCD com period 01: 1/8 LCD com period 10: 1/16 LCD com period 11: 1/32 LCD com period

3	LCDLDOEN	LCD 3V LDO Disable Control 0: Close (default) 1: Open, select LDO power supply, VLCD=3V, CONTR[2:0] invalid.
2-0	MOD[2:0]	Drive mode selector: 000: Traditional mode, bias resistor is 1.5Mk 001: Traditional mode, bias resistor is 900K 010: Traditional mode, bias resistor is 60k 011: fast charge up mode, bias resistor is switched between 60k and 900K automatic 1xx: fast charge up mode, bias resistor is switched between 60k and 1.5M automatic

Table 8.3 P4 fuction select register

FF80H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P4SS	P4S7	P4S6	P4S5	P4S4				
R/W	R/W	R/W	R/W	R/W				
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0				

Bit Number	Bit Mnemonic	Description
7-4	P4S[7:4]	P4 fuction select 0：P4.4-P4.7 as I/O 1：P4.4-P4.7 as LCD□，Segment which is controlled by COM which is controlled by DUTY[2:0]

Table 8.4 P5 fuction select register

FF81H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5SS	P5S7	P5S6	P5S5	P5S4	P5S3	P5S2	P5S1	P5S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-4	P5S[7:4]	P5 fuction select 0：P5.4-P5.7 as I/O 1：P5.4-P5.7 as LCD SEG
0	P5S[3:0]	P5 fuction select 0：P5.0-P5.3 as I/O 1：P5.0-P5.3 as Segment which is controlled by COM which is controlled by DUTY[2:0]

Table 8.5 P6 fuction select register

FF82H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P6SS	P6S7	P6S6	P6S5	P6S4	P6S3	P6S2	P6S1	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	-

Bit Number	Bit Mnemonic	Description
6-3	P6SS[7:1]	P6 fuction select 0：P6.0-P6.7 as I/O 1：P6.0-P6.7 as Segment

Table 8.6 P7 fuction select register

FF83H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P7SS	-	-	P7S5	-	-	-	P7S1	P7S0
R/W	-	-	R/W	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	0	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7-0	P7SS[7:0]	P7 fuction select 0：P7.0-P7.7 as I/O 1：P7.0-P7.7 as Segment

Table 8.7 P8 fuction select register

FF84H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P8SS	P8S7	P8S6	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	-	-	-	-

Bit Number	Bit Mnemonic	Description
7-0	P8S[7:6]	P8 fuction select 0：P8.0-P8.7 as I/O 1：P8.0-P8.7 as Segment

Table 8.8 P9 fuction select register

FF85H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P9SS	P9S7	P9S6	P9S9	P9S4	P9S3	P9S2	P9S1	P9S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	P9S[7:0]	P9 fuction select 0：P9.0-P9.7 as I/O 1：P9.0-P9.7 as LCD□，Segment or COM which is controlled by DUTY[2:0]

8.1.3 LCD RAM config

地址	7	6	5	4	3	2	1	0
	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1
2500H	-	-			SEG1	SEG1	SEG1	SEG1
2501H	-	-			SEG2	SEG2	SEG2	SEG2
2502H	-	-	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
2503H	-	-	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
2504H	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5
2505H	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
2506H	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
2507H	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
2508H	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
2509H	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
250AH	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
250BH	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
250CH	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
250DH	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
250EH	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
250FH	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16
2510H	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17
2511H	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18
2512H	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19
2513H	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20
2514H	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21
2515H	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22
2516H	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23
2517H	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24
2518H	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25
2519H	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26
251AH	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27
251BH	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28
251CH	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29
251DH	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30
251EH	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31
251FH	SEG32	SEG32	SEG32	SEG32	SEG32	SEG32	SEG32	SEG32
2520H	SEG33	SEG33	SEG33	SEG33	SEG33	SEG33	SEG33	SEG33
2521H	SEG34	SEG34	SEG34	SEG34	SEG34	SEG34	SEG34	SEG34
2522H	SEG35	SEG35	SEG35	SEG35	SEG35	SEG35	SEG35	SEG35
2523H	SEG36	SEG36	SEG36	SEG36	SEG36	SEG36	SEG36	SEG36
2524H	SEG37	SEG37	SEG37	SEG37	SEG37	SEG37	SEG37	SEG37
2525H	SEG38	SEG38	SEG38	SEG38	SEG38	SEG38	SEG38	SEG38
2526H	SEG39	SEG39	SEG39	SEG39	SEG39	SEG39	SEG39	SEG39
2527H	SEG40	SEG40	SEG40	SEG40	SEG40	SEG40	SEG40	SEG40

8.2 EUART

8.2.1 Features

The G80F975A has three enhanced EUART which build in a Baud-rate generator
The baud rate generator is a 15-bit up counter
Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
The EUART can be operated in four modes

8.2.2 EUART Mode Description

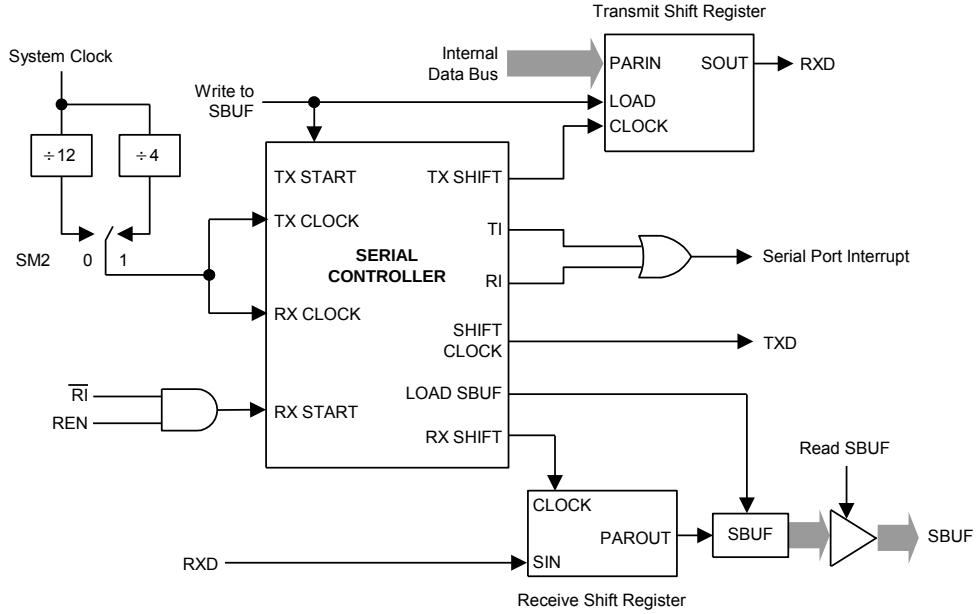
The EUART can be operated in 4 modes. Users must initialize the SCON before any communication can take place.
In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if RI = 0 and REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

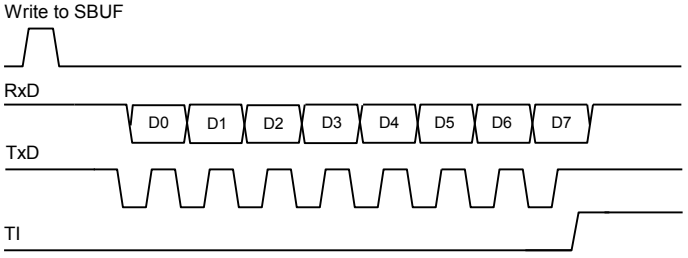
SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit
0	0	0	Sych	fSYS/ (4 or 12)	8 bits	NO	NO	None
0	1	1	Ansych	Built-in BaudRate generator overflow rate/16	10 bits	1	1	None
1	0	2	Ansych	fSYS/ (32 or 64)	11 bits	1	1	0, 1
1	1	3	Ansych	Built-in BaudRate generator overflow rate/16	11 bits	1	1	0, 1

Mode 0: Synchronous Mode, Half duplex

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RxD line. TxD is used to output the shift clock. The TxD clock is provided by the G80F975Awhether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first.
The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.
The functional block diagram is shown below. Data enters and exits the serial port on the RxD line. The TxD line is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the G80F975A

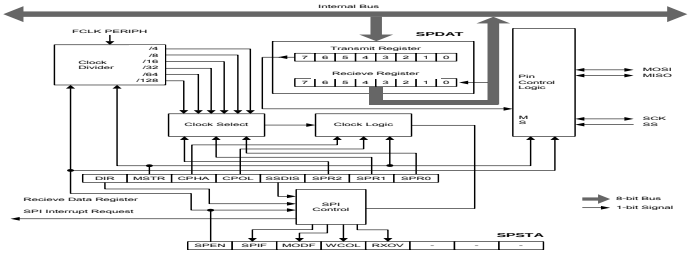


Any instruction that uses SBUF as a destination register (“write to SBUF” signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivates SEND and sets TI (SCON.1) at the rising edge of the next system clock.



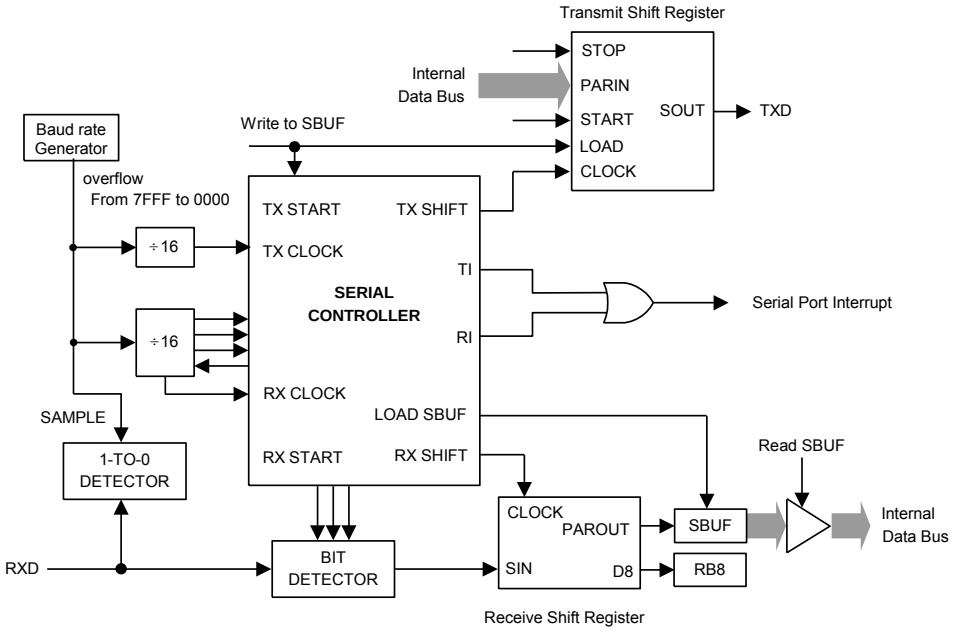
Send Timing of Mode 0

Reception is initiated by the condition REN (SCON.4)= 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivates RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.

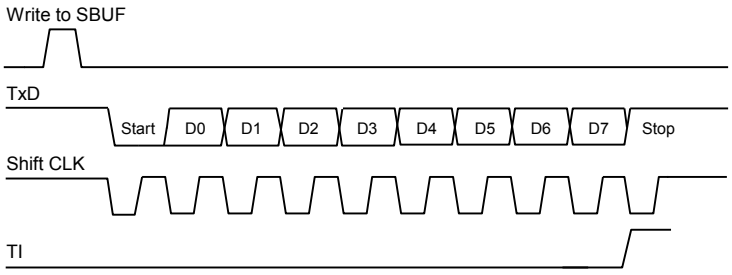


Mode 1: 8-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The baud rate in this mode is variable. The serial receive and transmit baud rate can be programmed to be 1/16 of the BaudRate generator overflow. The functional block diagram is shown below.

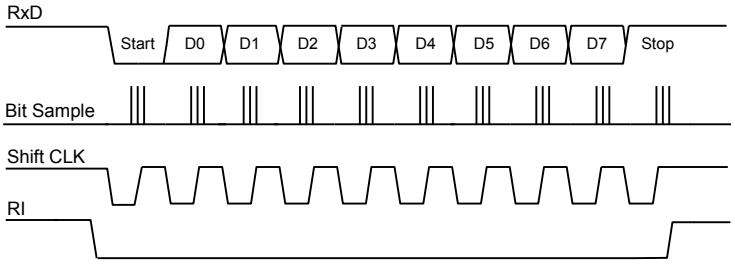


Transmission begins with a “write to SBUF” signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal. The start bit is firstly put out on TxD pin, then are the 8 bits of data. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time that the stop is send.



Send Timing of Mode 1

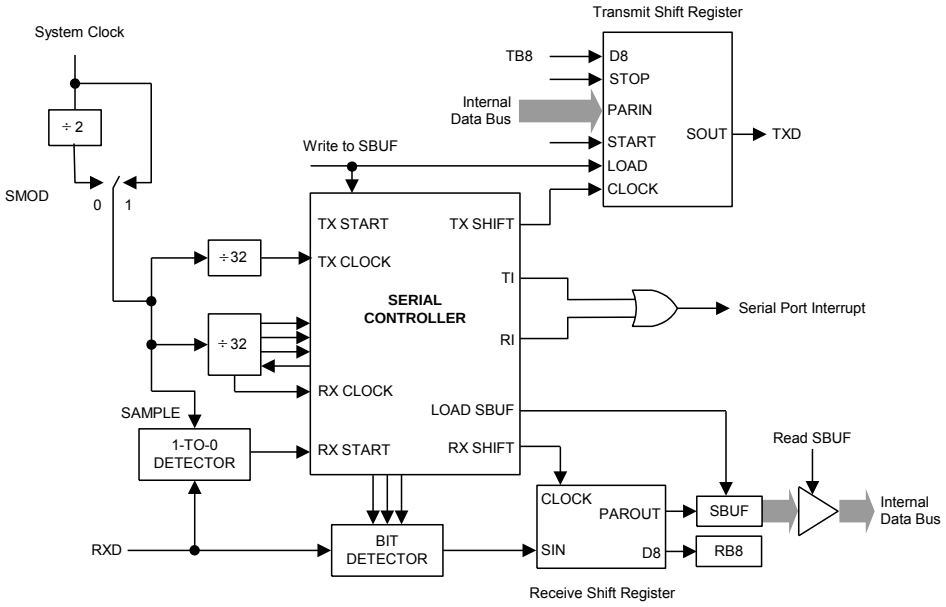
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7th, 8th and 9th counter states of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI are set if the following conditions are met:
RI must be 0
Either SM2 = 0, or the received stop bit = 1
If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



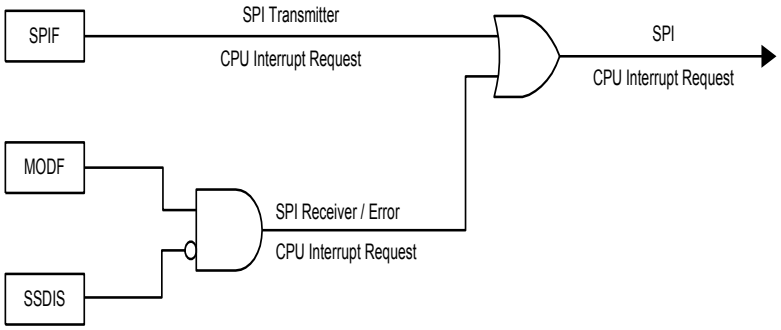
Receive Timing of Mode 1

Mode 2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

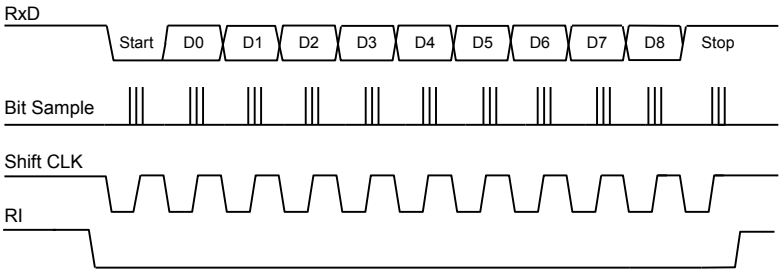
This mode provides the 11 bits full duplex asynchronous communication. The 11 bit consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition (Refer to Multiprocessor Communication Section for details). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, the “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal). The start bit is firstly put out on TxD pin, then are the 9 bits of data. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time, this will be at the 11th rollover of the divide-by-16 counter after a write to SBUF.



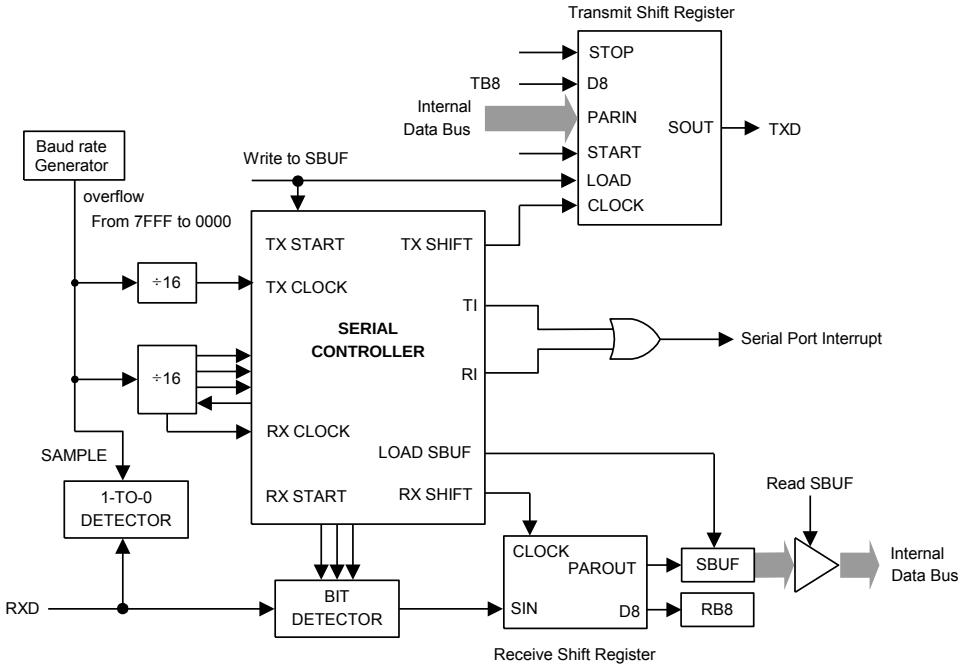
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter. The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7th, 8th and 9th counter state of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit detected after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register.
After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set if the following conditions are met:
RI must be 0
Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address
If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

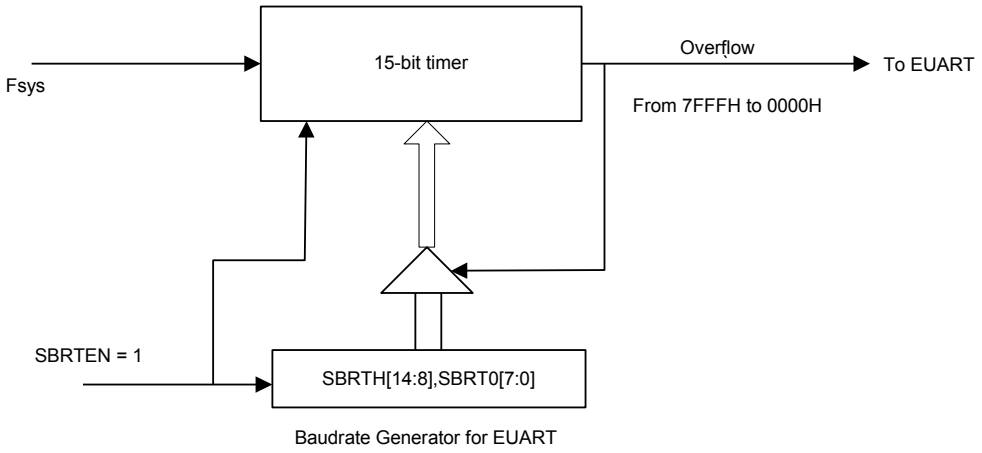
Mode 3: 9-Bit EUART, Variable Baud Rate, Asynchronous Full-Duplex

Mode 3 uses transmission protocol of the Mode 2 and baud rate generation of the Mode 1.



8.2.3 Baud rate Generator

EUART0, EUART1, EUART2 each carry a baudrate generator, It is essentially a 15-bit up counter.



Baudrate Generator for EUART

The baudrate is $SBRTover flowrate = \frac{Fsys}{32768 - SBRT}$, $SBRT = [SBRT1, SBRT0]$

so, the baud rate is calculated as follows in each mode.

In Mode 0, the baud rate is programmable system clock 1/12 or 1/4 determined by the SM2 bit. When SM2=0, the serial port to run under the system clock 1/12. When SM2 =1, the serial port 1/4 of the system clock run.

In mode 1 and 3, the baud rate can be fine fixed with accuracy of one system clock. The formula is shown below:

$$BaudRate = \frac{Fsys}{16 \times (32768 - SBRT) + BFINE}$$

E.G. When Fsys=8MHz, in order to generate a 11520Hz Baudrate, the value of SBRT and SFINE can be calculated from,
8000000/16/115200 = 4.34
SBRT = 32768 – 4 = 32764
115200 = 8000000/(16×4 + BFINE)
BFINE = 5.4 ≈ 5
The method with fine register comes into a 115942Hz Baudrate with 0.64% error compared to 8.5% error of calculating in old method.

In Mode 2, the baud rate is fixed for the system clock 1/32 or 1/64, determined by the SMOD bit (PCON.7). When the SMOD bit to 0, EUART to 1/64 of the system clock is running. When SMOD bit is 1, EUART run the system clock 1/32.

$$BaudRate = 2^{SMOD} \times (\frac{f_{SYS}}{64})$$

8.2.4 Multi-processor communication

Software address recognition

Modes 2 and 3 of the EUART have a special provision for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the EUART interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte.

With SM2 = 1, no other slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed leave their SM2 set and go on with their business, ignoring the incoming data bytes. Note:

In mode 0, SM2 is used to select baud rate doubling. In mode 1, SM2 can be used to check the validity of the stop bit. If SM2 = 1 in mode 1, the receive interrupt will not be activated unless a valid stop bit is received.

Automatic (Hardware) address recognition

In Mode 2 & 3, setting the SM2 bit will configure EUART0 act as following: when a stop bit is received, EUART0 will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART0 slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts on the reception of the following data byte(s).

The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the addressed slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the addressed slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, as they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all transmissions until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address.

Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. The slave address is an 8-bit value specified in the SADDR register. The SADEN register is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR. Use of the Given Address allows multiple slaves to be recognized while excluding others.

	Slave 1	Slave 2
SADDR	10100100	10100111
SADEN (0 mask)	11111010	11111001
Given Address	10100x0x	10100xx1
Broadcast Address (OR)	1111111x	11111111

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as don't cares. In most cases, the Broadcast Address is FFh, this address will be acknowledged by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXXXXXX (all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUART 0 will reply to any address, which it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor by software address recognition mentioned above.

8.2.5 EUART Error Detection

Error Detection

Error detection is available when the SSTAT bit in register PCON is set to logic 1.The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).All the 3 bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Transmit collision

The Transmit Collision bit (TXCOL bit in register SCON) reads '1' if RI is set 0 and user software writes data to the SBUF register while a transmission is still in progress. If this occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overrun

The Receive Overrun bit (RXOV in register SCON) reads '1' if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happen.

Frame Error

The Frame Error bit (FE in register SCON) reads '1' if an invalid (low) STOP bit is detected.

8.2.6 EUART0，1，3

EUART1/3 has the same control & operation modes as EUART0.

8.2.7 Registers

Table 8.9 Power Control register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	SSTAT1	SSTAT2	GF1	GF0	PD	IDL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SMOD	Baud rate doubler If set in mode 1 & 3, the baud-rate of EUART is doubled if using timer 1 as baud-rate generator, If set in mode 2, the baud-rate of EUART is doubled
6	SSTAT	SCON [7:5] function select bit 0： SCON [7:5] operates as SM0, SM1, SM2 1： SCON [7:5] operates as FE, RXOV, TXCOL
5	SSTAT1	SCON1 [7:5] function select bit 0： SCON1 [7:5] operates as SM10, SM11, SM12 1： SCON1 [7:5] operates as FE1, RXOV1, TXCOL1
4	SSTAT2	SCON1 [7:5] function select bit 0： SCON2 [7:5] operates as SM20, SM21, SM22 1： SCON2 [7:5] operates as FE2, RXOV2, TXCOL2
3-2	GF[1:0]	General purpose flags for software use
1	PD	Power-Down mode control bit
0	IDL	Idle mode control bit

Note: EUART3 SCON2 [7:5] is fixed as SM20，SM21，SM22

EUART0 SFR

Table 8.10 EUART0 Control & status Register

98H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0 /FE	SM1 /RXOV	SM2 /TXCOL	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	SM[0:1]	EUART0 Serial mode control, when SSTAT = 0 00 = mode 0, Synchronous Mode, fixed baud rate 01 = mode 1, 8 bit Asynchronous Mode, variable baud rate 10 = mode 2, 9 bit Asynchronous Mode, fixed baud rate 11 = mode 3, 9 bit Asynchronous Mode, variable baud rate
7	FE	EUART0 Frame Error flag, when SSTAT = 1 0 = No Frame Error, clear by software 1 = Frame error occurs, set by hardware
6	RXOV	EUART0 Receive Over flag, SSTAT = 1 0 = No Receive Over, clear by software 1 = Receive over occurs, set by hardware
5	SM2	EUART0 Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0 0 = In mode 0, baud-rate is 1/12 of system clock In mode 1, disable stop bit validation check, any stop bit will set RI to generate interrupt In mode 2 & 3, any byte will set RI to generate interrupt 1 = In mode 0, baud-rate is 1/4 of system clock In mode 1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In mode 2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	TXCOL	EUART0 Transmit Collision flag, SSTAT = 1 0 = No Transmit Collision, clear by software 1 = Transmit Collision occurs, set by hardware
4	REN	EUART0 Receiver enable. 0 = Receive Disable 1 = Receive Enable
3	TB8	The 9th bit to be transmitted in mode 2 & 3 of EUART0, set or clear by software
2	RB8	Transmitter bit 8 of EUART0 In mode 0, RB8 is not used. In mode 1, if receive interrupt occurs, RB8 is the stop bit that was received. In modes 2 & 3 it is the 9th bit that was received.
1	TI	Transmit interrupt flag of EUART0 0 = cleared by software. 1 = Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in other modes.
0	RI	Receive interrupt flag of EUART0 0 = cleared by software. 1 = Set by hardware at the end of the 8th bit time in mode 0, or during the stop bit time in other modes

Table 8.11 EUART0 Data buffer register

99H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SBUF[7:0]	This SFR accesses two registers; a transmit shift register and a receive latch register. A write of SBUF will send the byte to the transmit shift register and then initiate a transmission A read of SBUF returns the contents of the receive latch

Table 8.12 EUART0 Slave Address & Address Mask register

9AH-9BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR (9AH)	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN (9BH)	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SADDR[7:0]	SFR SADDR defines the EUART's slave address.
7-0	SADEN[7:0]	SFR SADEN is a bit mask to determine which bits of SADDR are checked against a received address: 0 : Corresponding bit in SADDR is a "don't care" 1 : Corresponding bit in SADDR is checked against a received address

Table 8.13 EUART0 Baud rate generator

9CH-9DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRTH (9CH)	SBRTEN	SBRT0.14	SBRT0.13	SBRT0.12	SBRT0.11	SBRT0.10	SBRT0.9	SBRT0.8
SBRTL (9DH)	SBRT0.7	SBRT0.6	SBRT0.5	SBRT0.4	SBRT0.3	SBRT0.2	SBRT0.1	SBRT0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SBRTEN	EUART0 Baud rate generator control: 0：disable（default） 1：enable
6-0 7-0	SBRT[14:0]	EUART0 Baud rate generator counter high 7/8-bit

Table 8.14 EUART0/1 baudrate generator fine register

9EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SFINE	SFINE.3	SFINE.2	SFINE.1	SFINE.0	SFINE.3	SFINE.2	SFINE.1	SFINE.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	SFINE[3:0]	EUART1/0 baudrate generator fine data register

EUART1 SFR

Table 8.15 EUART1 Control & status Register

D8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON1	SM10 /FE1	SM11 /RXOV1	SM12 /TXCOL1	REN1	TB18	RB18	TI1	RI1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	SM1[0:1]	EUART1 Serial mode control bit, when SSTAT1 = 0 00 : mode 0, Synchronous Mode, fixed baud rate 01 : mode 1, 8 bit Asynchronous Mode, variable baud rate 10 : mode 2, 9 bit Asynchronous Mode, fixed baud rate 11 : mode 3, 9 bit Asynchronous Mode, variable baud rate
7	FE1	EUART1 Frame Error flag, when FE1 bit is read, SSTAT1 bit must be set 1 0 : No Frame Error, clear by software 1 : Frame error occurs, set by hardware
6	RXOV1	EUART1 Receive Over flag, when RXOV1 bit is read, SSTAT1 bit must be set 1 0 : No Receive Over, clear by software 1 : Receive over occurs, set by hardware
5	SM12	EUART1 Multi-processor communication enable bit (9th bit '1' checker), when SSTAT1 = 0 0 : In mode 0, baud-rate is 1/12 of system clock In mode 1, disable stop bit validation check, any stop bit will set RI1 to generate interrupt In mode 2 & 3, any byte will set RI1 to generate interrupt 1 : In mode 0, baud-rate is 1/4 of system clock In mode 1, Enable stop bit validation check, only valid stop bit (1) will set RI1 to generate interrupt In mode 2 & 3, only address byte (9th bit = 1) will set RI1 to generate interrupt
5	TXCOL1	EUART1 Transmit Collision flag, when TXCOL bit is read, SSTAT1 bit must be set 1 0 : No Transmit Collision, clear by software 1 : Transmit Collision occurs, set by hardware
4	REN1	EUART1 Receiver enable bit 0 : Receive Disable 1 : Receive Enable
3	TB81	The 9th bit to be transmitted in mode 2 & 3 of EUART1, set or cleared by software
2	RB81	The 9th bit to be received in mode 1,2 & 3 of EUART In mode 0, RB18 is not used In mode 1, if receive interrupt occurs, RB18 is the stop bit that was received In modes 2 & 3 it is the 9th bit that was received
1	TI1	Transmit interrupt flag of EUART1 0 : cleared by software 1 : Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in other modes
0	RI1	Receive interrupt flag of EUART1 0 : cleared by software 1 : Set by hardware at the end of the 8th bit time in mode 0, or during the stop bit time in other modes

Table 8.16 EUART1 Data buffer register

D9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF1	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SBUF1[7:0]	This SFR accesses two registers; a transmit shift register and a receive latch register. A write of SBUF1 will send the byte to the transmit shift register and then initiate a transmission A read of SBUF1 returns the contents of the receive latch.

Table 8.17 EUART1 Slave Address & Address Mask register

DAH-DBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR1 (DAH)	SADDR1.7	SADDR1.6	SADDR1.5	SADDR1.4	SADDR1.3	SADDR1.2	SADDR1.1	SADDR1.0
SADEN1 (DBH)	SADEN1.7	SADEN1.6	SADEN1.5	SADEN1.4	SADEN1.3	SADEN1.2	SADEN1.1	SADEN1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SADDR1[7:0]	SFR SADDR1 defines the EUART's slave address.
7-0	SADEN1[7:0]	SFR SADEN1 is a bit mask to determine which bits of SADDR are checked against a received address: 0 : Corresponding bit in SADDR1 is a "don't care". 1 : Corresponding bit in SADDR1 is checked against a received address.

Table 8.18 EUART1 Baud rate generator

DCH-DDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRT1H (DCH)	SBRTEN1	SBRT1.14	SBRT0.13	SBRT0.12	SBRT0.11	SBRT0.10	SBRT0.9	SBRT1.8
SBRT1L (DDH)	SBRT1.7	SBRT1.6	SBRT1.5	SBRT1.4	SBRT1.3	SBRT1.2	SBRT1.1	SBRT1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SBRTEN1	EUART1 Baud rate generator control: 0：disable（default） 1：enable
6-0 7-0	SBRT1[14:0]	EUART1 Baud rate generator counter high 7/8-bit

EUART3 SFR

Table 8.24 EUART2 Control & status Register

FFD0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON3	SM30	SM31	SM33	REN3	TB38	RB38	TI3	RI3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	SM3[0:1]	EUART3 Serial mode control bit, when SSTAT2 = 0 00 : mode 0, Synchronous Mode, fixed baud rate 01 : mode 1, 8 bit Asynchronous Mode, variable baud rate 10 : mode 2, 9 bit Asynchronous Mode, fixed baud rate 11 : mode 3, 9 bit Asynchronous Mode, variable baud rate
5	SM22	EUART3 Multi-processor communication enable bit (9th bit '1' checker), when SSTAT2 = 0 0 : In mode 0, baud-rate is 1/12 of system clock In mode 1, disable stop bit validation check, any stop bit will set RI1 to generate interrupt In mode 2 & 3, any byte will set RI1 to generate interrupt 1 : In mode 0, baud-rate is 1/4 of system clock In mode 1, Enable stop bit validation check, only valid stop bit (1) will set RI1 to generate interrupt In mode 2 & 3, only address byte (9th bit = 1) will set RI1 to generate interrupt
4	REN3	EUART3 Receiver enable bit 0 : Receive Disable 1 : Receive Enable
3	TB83	The 9th bit to be transmitted in mode 2 & 3 of EUART3, set or cleared by software
2	RB83	The 9th bit to be received in mode 1,2 & 3 of EUART3 In mode 0, RB18 is not used In mode 1, if receive interrupt occurs, RB18 is the stop bit that was received In modes 2 & 3 it is the 9th bit that was received
1	TI3	Transmit interrupt flag of EUART3 0 : cleared by software 1 : Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in other modes
0	RI3	Receive interrupt flag of EUART3 0 : cleared by software 1 : Set by hardware at the end of the 8th bit time in mode 0, or during the stop bit time in other modes

Notes:

TI3，RI3 can only be cleared.，"READ-MODIFY-WRITE" instructions (like logic operation instructions) aren't allowed to the 2 bits

Table 8.25 EUART3 Data buffer register

FFD1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF3	SBUF3.7	SBUF3.6	SBUF3.5	SBUF3.4	SBUF3.3	SBUF3.3	SBUF3.1	SBUF3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SBUF3[7:0]	This SFR accesses two registers; a transmit shift register and a receive latch register. A write of SBUF1 will send the byte to the transmit shift register and then initiate a transmission A read of SBUF1 returns the contents of the receive latch.

Table 8.26 EUART3 Slave Address & Address Mask register

FFD2H-FFD3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR3 (FFD2H)	SADDR3.7	SADDR3.6	SADDR3.5	SADDR3.4	SADDR3.3	SADDR3.3	SADDR3.1	SADDR3.0
SADEN3 (FFD3H)	SADEN3.7	SADEN3.6	SADEN3.5	SADEN3.4	SADEN3.3	SADEN3.3	SADEN3.1	SADEN3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SADDR3[7:0]	SFR SADDR3 defines the EUART3's slave address.
7-0	SADEN3[7:0]	SFR SADEN3 is a bit mask to determine which bits of SADDR are checked against a received address: 0 : Corresponding bit in SADDR1 is a "don't care". 1 : Corresponding bit in SADDR1 is checked against a received address.

Table 8.27 EUART3 Baud rate generator

FFD4H-FFD5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRT3H (FFD4H)	SBRTEN3	SBRT3.14	SBRT3.13	SBRT3.13	SBRT3.11	SBRT3.10	SBRT3.9	SBRT3.8
SBRT3L (FFD5H)	SBRT3.7	SBRT3.6	SBRT3.5	SBRT3.4	SBRT3.3	SBRT3.3	SBRT3.1	SBRT3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SBRTEN3	EUART3 Baud rate generator control: 0：disable（default） 1：enable
6-0 7-0	SBRT3[14:0]	EUART3 Baud rate generator counter high 7/8-bit

8.3 infrared transmission/acceptance interface.

G80F975A provides a built-in IR transmission module that can modulated the TXD output signal of EUART to drive the infrared transmitting tube and the iTXD output 0.

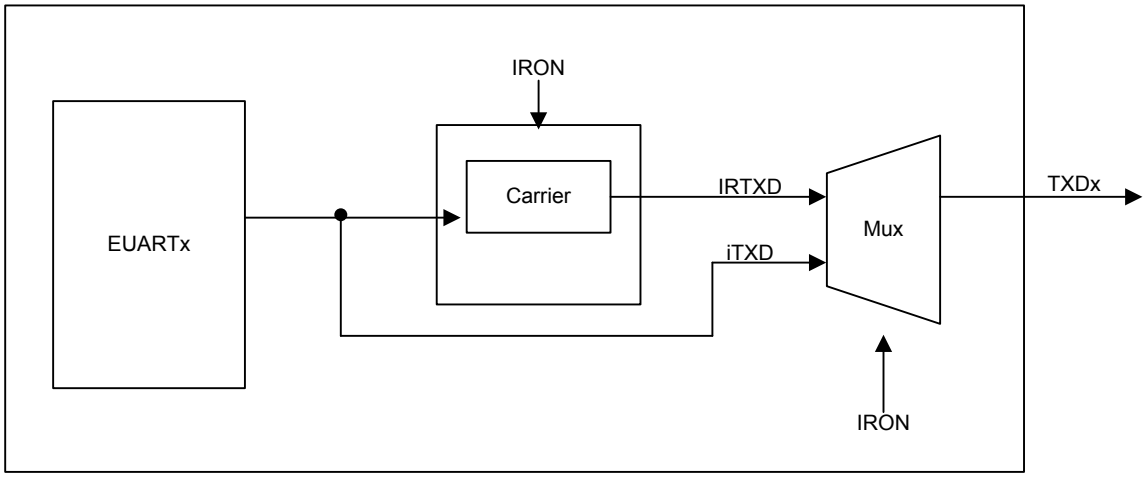
In the case of IRTXD modulation, the IR transmission module modulates the carrier of a particular frequency.

IRF register determines the carrier frequency. Each carrier is synchronized with the falling edge of with TXD1 signal.

When the increase of IR carrier, in order to EUART1 error reduced to the smallest, the baud rate is lower than 9600bps.

IR delivery module by Registers can and can only be used with one of the four EUART carrier frequency computation formula is as follows:

$$F_{carrier} = \frac{SYSCLK}{2 \times (IRF + 1)}$$



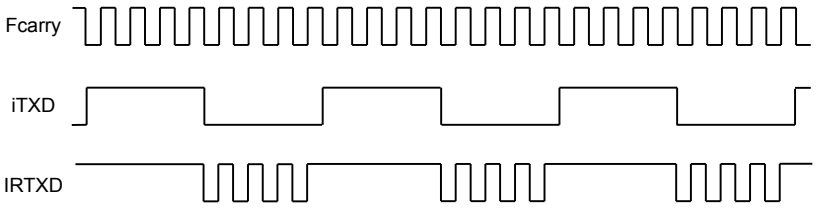


Table 8.28 IR control register

ADH,AEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRCON1(ADH)	IRON	IRS	-	-	IRF11	IRF10	IRF9	IRF8
IRDAT(AEH)	IRF7	IRF6	IRF5	IRF4	IRF3	IRF2	IRF1	IRF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （POR/WDT /LVR/PIN）	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	IRON	IR control : 0: disable IR, EUART1 as I/O 1: enable IR, IR frequency load EUART1 TxD signal
6	IRS	IR output polarity control bit. 0：Higher output，When iTXD=1，TXDx output 1；when iTXD=0，TXDx output carrier 1：Reverse output，When iTXD=1，TXDx output carrier；when iTXD=0，TXDx output 0
3-0 7-0	IRF [11：0]	IR carrier frequency selective high four Registers

Table 8.29 IR control register 2

AFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

IRCON2	-	-	-	-	-	-	IRSEL1	IRSEL0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1-0	IRSEL[1:0]	IR carrier transmission selector. 00: IR carrier is connected to EUART0. 01: IR carrier is connected to EUART1. 10: IR carrier is connected to EUART2. 11: IR carrier is connected to EUART3.

8.4 ADC

8.4.1 feature

14-bit resolution

Built-in reference voltage

8 analog channel input

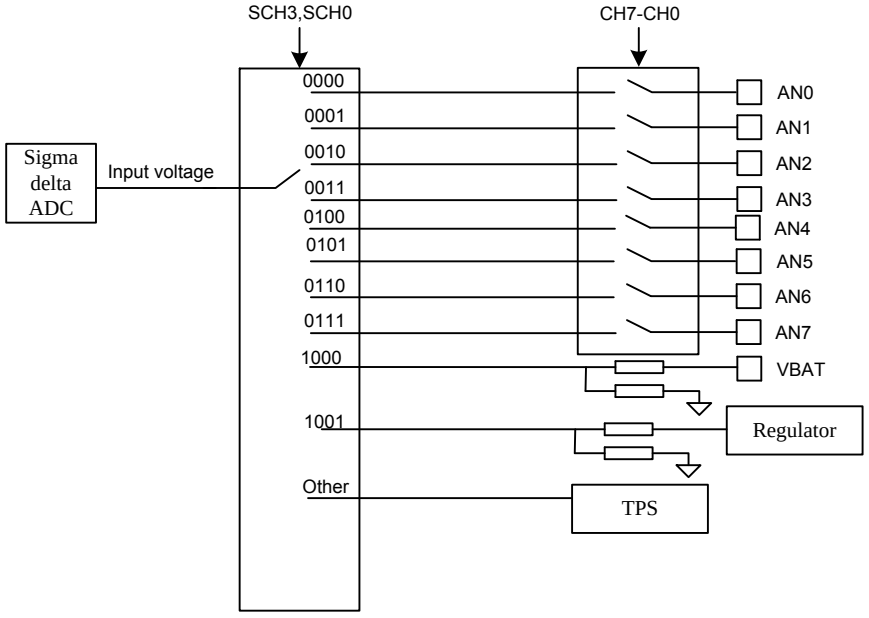
The . G80F975A include a single ended

Includes a single-ended sigma-detla number/mode converter，ADC build in reference voltage VREF1.2V， 8 ADC channels are share with one ADC module, each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. GO/$\overline{\text{DONE}}$ signal is available to start convert, and indicate end of convert. When onversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCON register will be set to generate an interrupt if ADC Interrupt is enabled.

The ADC USES a 2.8v regulator inside the chip and USES the 8MHz RC oscillator as the clock source, so it can work in Idle mode and power-down mode.

The ADC has three channels for measuring internal signals in the chip, VCC(1.55V regulator), VBAT and temperature sensors. As a result of the ADC reference voltage is 1.2 V, so to be more than the voltage of the channel input, need to fall below 1.2 V the sampling signal and measured again, within the internal signal VBAT and VCC has partial pressure resistance, electric subsection compression ratio of 1:5 (partial pressure resistance 5 k / 25 k), only when the switch are VBAT, VCC, partial pressure resistance to sub

8.4.2 ADC Diagram



ADC Block Diagram

8.4.3 Registers

Table 8.26 ADC Control Register

C1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	TPSCON	SCH3	SCH2	SCH1	SCH0	GO/$\overline{DONE}$
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	ADON	ADC Enable 0 = Disable the ADC module 1 = Enable the ADC module
6	ADCIF	ADC Interrupt Flag 0 = No ADC interrupt, cleared by software. 1 = Set by hardware to indicate that the AD Convert has been completed,
5	TPSCON	Temperature measurement module allows. 0: Temperature measurement module is prohibited. 1: Allow temperature measurement module.
4-1	SCH[3:0]	ADC channel Select 0000: ADC channel AN0 0001: ADC channel AN1 0010: ADC channel AN2 0011: ADC channel AN3 0100: ADC channel AN4 0101: ADC channel AN5 0110: ADC channel AN6 0111: ADC channel AN7 1000：Battery 1001：Internal VBG other:TPS
0	GO/$\overline{DONE}$	ADC status flag 0 = Automatically cleared by hardware when AD convert is completed. Clearing this bit during converting time will stop current conversion. 1：Set to start AD convert.

Table 8.27 ADC Channel Configure Register

C2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	ADCCLK1	ADCCLK0	ADCM	-	-	-	CICCTL1	CICCTL0
R/W	R/W	R/W	R/W	-	-	-	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	1	1	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7-6	ADCCLK[1:0]	Temperature sensor /ADC clock source selection. 00: 330K 01: 165K(default) 1x: 82.5K

5	ADCM	ADC modulator option. 0: mode A 1: mode B(default)
1-0	CICCTL[1:0]	channel Configuration 00: CIC drop sampling 16384(ADC conversion result is 14 bits.，Convert time to 295ms) 01: CIC drop sampling 8192(ADC conversion result is 13.，Convert time to 148ms) 10: CIC drop sampling 2048(ADC conversion result is 11 bits.，Convert time to 37ms) 11: CIC drop sample 1024(ADC conversion result is 10 bits.，Convert time to 18.5ms)

Table 8.28 ADC Channel Configure Register

C3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	CH[7:0]	Channel Configuration 0：P2.5-P1.6 as standard I/O port 1：P2.5-P1.6 as ADC input, if no other function in use

Table 8.29 AD converter Data register

C4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDL	A7	A6	A5	A4	A3	A2	A1	A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0
C5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDH	-	-	A13	A12	A11	A10	A9	A8
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	-	-	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
5-0 7-0	A13-A0	ADC data register: Digital Value of sampled analog voltage, updated when conversion is completed

The Approach for AD Conversion:
(1) enable 2.8V LDO
(2) Select the analog input channels and reference voltage.
(3) Enable the ADC module with the selected analog channel.
(4) Set GO/$\overline{\text{DONE}}$ = 1 to start the AD conversion.
(5) Wait until GO/$\overline{\text{DONE}}$ = 0 or ADCIF = 1, if the ADC interrupt is enabled, the ADC interrupt will occur.
(6) Acquire the converted data from ADDH/ADDL.
(7) Repeat step 4-6 if another conversion is required.

Start temperature conversion steps:
(1) enable temperature sensor module.
(2) Waiting for the 200us
(3) Set up the correct adc channel.
(4)GOS/$\overline{\text{DONE}}$S set 1 to start the temperature sensor conversion.
(5) Waiting for the GOS/$\overline{\text{DONE}}$S=0 or ADCIF =1, If the ADC interrupts enable, the ADC interrupt will be generated and the user needs the software to clear 0.
(6) The conversion data is obtained from ADDH/ADDL.
(7) Repeat steps 4 ~ 6 to start another conversion.

8.4.4 Temperature offsetRegisters
G80F975A each chip will be cured with the temperature of the RegistersTEMPBL, TEMPBH, TEMPKL and TEMPKH values，It can't be erased, can be read by program or programming tool.
The sample is as follows：

```
unsigned char code *ptr;
unsigned char flashconbak, tempbl, tempbh,tempkl,tempkh;
flashconbak = FLASHCON;
FLASHCON=0x01;
ptr =(unsigned char code *) 0x1228;
tempbl = *ptr;
ptr = (unsigned char code *)0x1229;
tempbh = *ptr;
ptr = (unsigned char code *)0x122A;
tempkl = *ptr;
ptr = (unsigned char code *)0x122B;
tempkh = *ptr;
FLASHCON= flashconbak;
```

The formula for calculating the temperature.

```
T = (float)(TEMPKH*256+TEMPKL)/100000*((int)(ADCH*256+ADCL)+(int)(TEMPBH*256+TEMPBL))
```

8.5 RTC (Real Timer Clock)

8.5.1 Features

32.768kHz clock input with frequency compensation.
Built-in high-precision frequency compensation circuit, compensation accuracy: 0.127PPM.
Counter registers for: Half second, Second, Minute, Hour, Day, Day-of-week, Month, Year
Day counter with automatic month and leap year adjustment
Provides two Real Time Clock Alarms and a Timer.
Provides the accurate seconed pulse output.

8.5.2 Functional Description

Time & Calendar function:

The RTC module provides clock indications in seconds, minutes, and hours; calendar indications in day-of-week, day-of-month, month, and year(four-year calendar) with automatic adjustment for month and leap year. Reading the clock and calendar registers return the current time and date. Writing to these registers set the time and date, and the counters will continue to count from the new settings.

Calendar functions are provided by the day, day-of-week, month, and year counter registers. The roll over of the day counter is automatically adjusted for the month and leap years.

Cycle length of the time RTC

Registers	COUNTING CYCLE	CARRY TO NEXT UNIT	COMMENT
SBSC	00-255	255→0	SBSC overflow, SEC plus 1
SEC	00-59	59→00	-
MIN	00-59	59→00	-
HR	00-23	23→00	-
DAY	01-31	31→01	MTH=1,3,5,7,8,10 and 12
	01-30	30→01	MTH=4,6,9 and 11
	01-29	29→01	MTH=2, YR=0 (leap year)
	01-28	28→01	MTH=2, YR=1,2 and 3
MTH	01-12	12→01	-
YR	0-99	99→0	YR=0, leap year
DOW	0-6	6→0	-

SCBC's value is equal to high 8 bit of 1 Hz frequency divider (source from 32.768KHz). Write 0x00 to SCBC will clear the high 8 bit register of divider. So SCBC also can be used for correcting time difference.

Read the calendar registers

RTCCRD is used for reading time. When RTCRD = 0, the time register update by frequency 32768 Hz. When RTCRD = 1, the newest time data update to register and stop refresh register until set RTCRD = 0 again.

Write the calendar registers

Step 1: set RTCWD = 0x69. This step will stop the update of time registers and make this registers (include RTCPSW) writable.
Step 2: write data to time registers.
Step 3: set RTCPSW = 0x5a. This step will check the data you write. When the data is under rule of each register, write success and clear RTCPSW. When the data is illegal, cancel write operation and set RTCPSW = 0x01.

Compensation

A frequency compensation mechanism is built into this RTC module to allow adjustments to the RTC clock when a less accurate 32.768kHz crystal is used. With the compensation mechanism, a more accurate real time could be made than the frequency accuracy of the crystal that drives the module. The compensation value can be be set by application software, the compensation cycle is 60s (high frequency compensaton second pulse's compensaton cycle is 1s).1 LSB of compensaton register can correct 0.127 PPM (1/60/32768/4) frequency error. There are 13 bit register (two's complement) use for compensation, and higest bit reflect the polarity (0 means the crystal is too fast, 1 means the crystal is too slow). The compensation range is -1024PPM to 1024PPM. The relation of frequency error (Err, Unit:S/D) and compensaton value (E) as follow:

Err > 0 E(13:0) = Err * 11.574 / 0.127
Err < 0 E(13:0) = ~(|Err| * 11.574 / 0.127) + 1

Alarm Function

Built-in 2 group alarm, one group include Second, Minute, Hour, Day, Day-of-week alarm register, the other one include Second, Minute, Hour alarm register. When the time register data equal the alarm register, ALM0(1) be set to 1 and alarm interrupt generate (when alarm interrupt is enabled). At the same time, if OUTF[1:0] = 11, alarm 1 will output a 80ms(±1ms) pulse in CALOUT.

ALMCON use to enable or disable each alarm register, There is no rule set to check the alarm register data, but the wrong data may cause unexpected result. Therefore, take care in software programming.

Timer Function

Build-in 8 bit timer, the timer's clock source can be choose by set ITS[1:0]. ITEN is a bit to control disable/enable timer function. When the timer overflow, the timer register (RTCTMR) auto reload, set ITIF = 1, generate timer interrupt (if the interrupt is enabled).

Interrupt Function

Provides second, minute, hour interrupt and alarm, timer interrupt. Each interrupt include interrupt control bit and interrupt flag bit, the interrupt flag can be set 1 by hardware and clear by software

IO Pin

The RTC function uses 1 I/O pin: CALOUT. CALOUT is controlled by output control register OUTF, CALOUT output pin for: compensated clock output after calibration, which can be programmed to output compensated 60-second clock or its original 32KHz clock, period changing signal. The output polarity can be set by OUTS

8.5.3 Registers

Table 8.34 RTC subsecond register

FFA0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBSC	SBSC7	SBSC6	SBSC5	SBSC4	SBSC3	SBSC2	SBSC1	SBSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	*	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
7-0	SBSC[7:0]	RTC Subsecond Value This register (bit0 ~ bit7) contains the current value of the high 8 bit of 1 Hz divider. This register (bit0 ~ bit7) can be read at any time without affecting the counter count. Writing to this register (bit0 ~ bit7) loads the value to the subsecond counter and the counter continues to count from this new value. The subsecond counter rolls over to 0 after reaching 255.

NOTE: * : means random value .

Table 8.35 Second Register

FFA1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEC	-	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	*	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
6-0	SEC[6:0]	This register (bit0 ~ bit6) contains the current value (BCD) of the second counter. This register (bit0 ~ bit6) can be read at any time without affecting the counter count. Writing to this register (bit0 ~ bit6) loads the value to the second counter and the counter continues to count from this new value. The second counter rolls over to 0 after reaching 59. Writing a value other than 0 to 59 to this register has no effect. Be sure not to write a data such as '0x, 1x, 2x, 3x, 4x (x=A~F)' to this register.

Table 8.36 Minute Register

FFA2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MIN	-	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
6-0	MIN[6:0]	This read/write register contains the current value (BCD) of the minute counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the minute counter and the counter continues to count from this new value. The minute counter rolls over to 0 after reaching 59. Writing a value other than 0 to 59 to this register has no effect. Be sure not to write a data such as '0x, 1x, 2x, 3x, 4x (x=A~F)' to this register.

Table 8.37 Hour Register

FFA3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HR	-	-	HR5	HR4	HR3	HR2	HR1	HR0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	-	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
5-0	HR[5:0]	This read/write register contains the current value (BCD) of the hour counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the hour counter and the counter continues to count from this new value. The hour counter rolls over to 0 after reaching 23. Writing a value other than 0 to 23 to this register has no effect. Be sure not to write a data such as '0x, 1x (x=A~F)' to this register.

Table 8.38 Day Register

FFA4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DAT	-	-	DAY5	DAY4	DAY3	DAY2	DAY1	DAY0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	-	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
5-0	DAY[5:0]	This read/write register contains the current value (BCD) of the day-of-month counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the day counter and the counter continues to count from this new value. The day counter rolls over to 1 ($01) after reaching 28, 29 , 30 , or 31 , depending on the value in the month and year registers. Writing a value that is not valid for the month and year to this register has no effect. Be sure not to write a data such as '1x, 2x (x=A~F)' to this register.

Table 8.39 Month Register

FFA5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MTH	-	-	-	MTH4	MTH3	MTH2	MTH1	MTH0
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	-	-	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	-	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
4-0	MTH[4:0]	This read/write register contains the current value (BCD) of the month counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the month counter and the counter continues to count from this new value. The month counter rolls over to 1 after reaching 12 . Writing a value other than 1 to 12 to this register has no effect. Be sure not to write a data such as 'x (x=A~F)' to this register.

Table 8.40 Year Register

FFA6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
YR	YR7	YR6	YR5	YR4	YR3	YR2	YR1	YR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	*	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
7-0	YR[7:0]	This read/write register contains the current value (BCD) of the year counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the year counter and the counter continues to count from this new value. The YR value rolls over to 0 after reaching 99. Writing a value other than 0 to 99 to this register has no effect.

Table 8.41 Week Register

FFA7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOW	-	-	-	-	-	DOW2	DOW1	DOW0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value(POR)	-	-	-	-	-	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	-	-	-	u	u	u

Bit Number	Bit Mnemonic	Description
2-0	DOW[2:0]	This read/write register contains the current value (BCD) of the day-of-week counter. This register can be read at any time without affecting the counter count. Writing to this register loads the value to the day-of-week counter and the counter continues to count from this new value. The day-of-week counter value rolls over to 0 after reaching 6. Writing a value other than 0 to 6 to this register has no effect.

Table 8.42 RTC Compensation Value Register(E)

FFA8H-FFA9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCDATH (FFA8H)	-	-	E13	E12	E11	E10	E9	E8
RTCDATL (FFA9H)	E7	E6	E5	E4	E3	E2	E1	E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	0	0	*	*	*	*	*	*
	0	0	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	u	u	u	u	u	u
	-	-	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
7-0	E[13:0]	RTC Compensaton value (E) E[13:0] compensation value is the compensate clock number of RTC. E > 0 : Cut down E clock in a compensate cycle; E < 0 : Add E clock in a compensate cycle. E[13:0]: signed number expressed by two's complement. NOTE: Reset will not change this register’s value.

Table 8.43 RTC Alarm Control Register

FFAAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCALM	ALM1C2	ALM1C1	ALM1C0	ALM0C4	ALM0C3	ALM0C2	ALM0C1	ALM0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	*	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
7	ALM1C2	Alarm 1 Hour Enable bit 0：A1HR is not used as comparison data for generating an alarm 1：A1HR is used as comparison data for generating an alarm
6	ALM1C1	Alarm 1 Minute Enable bit 0：A1MIN is not used as comparison data for generating an alarm 1：A1MIN is used as comparison data for generating an alarm
5	ALM1C0	Alarm 1 Hour Enable bit 0：A1HR is not used as comparison data for generating an alarm 1：A1HR is used as comparison data for generating an alarm
4	ALM0C4	Alarm 0 Week Enable bit 0：A0DOW is not used as comparison data for generating an alarm 1：A0DOW is used as comparison data for generating an alarm
3	ALM0C3	Alarm 0 Day Enable bit 0：A0DAY is not used as comparison data for generating an alarm 1：A0DAY is used as comparison data for generating an alarm
2	ALM0C2	Alarm 0 Hour Enable bit 0：A0HR is not used as comparison data for generating an alarm 1：A0HR is used as comparison data for generating an alarm
1	ALM0C1	Alarm 0 minute Enable bit 0：A0MIN is not used as comparison data for generating an alarm 1：A0MIN is used as comparison data for generating an alarm
0	ALM0C0	Alarm 0 Second Enable bit 0：A0SEC is not used as comparison data for generating an alarm 1：A0SEC is used as comparison data for generating an alarm

Table 8.44 Alarm 0 Second Register

FFABH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0SEC	-	A0SEC6	A0SEC5	A0SEC4	A0SEC3	A0SEC2	A0SEC1	A0SEC0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
6-0	A0SEC[6:0]	Alarm 0 second register (BCD). When ALM0C0 = 1, second register (SEC) equal A0SEC and the other enabled alarm 0 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.45 Alarm 0 Minute Register

FFACH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0MIN	-	A0MIN6	A0MIN5	A0MIN4	A0MIN3	A0MIN2	A0MIN1	A0MIN0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
6-0	A0MIN[6:0]	Alarm 0 minute register (BCD). When ALM0C1 = 1, minute register (MIN) equal A0MIN and the other enabled alarm 0 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.46 Alarm 0 Hour Register

FFADH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0HR	-	-	A0HR5	A0HR4	A0HR3	A0HR2	A0HR1	A0HR0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	-	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
5-0	A0HR[5:0]	Alarm 0 hour register (BCD). When ALM0C2 = 1, hour register (HR) equal A0HR and the other enabled alarm 0 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.◦

Table 8.47 Alarm 0 Day Register

FFAEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0DAY	-	-	A0DAY5	A0DAY4	A0DAY3	A0DAY2	A0DAY1	A0DAY0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	-	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description

5-0	DAY[5:0]	Alarm 0 day register (BCD). When ALM0C3 = 1, day register (DAY) equal A0DAY and the other enabled alarm 0 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.48 Alarm 0 Week Register

FFAFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0DOW	-	-	-	-	-	A0DOW2	A0DOW1	A0DOW0
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value(POR)	-	-	-	-	-	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	-	-	-	u	u	u

Bit Number	Bit Mnemonic	Description
2-0	DOW[2:0]	Alarm 0 week register (BCD). When ALM0C4 = 1, week register (DOW) equal A0DOW and the other enabled alarm 0 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.49 Alarm 1 Second Register

FFB0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1SEC	-	A1SEC6	A1SEC5	A1SEC4	A1SEC3	A1SEC2	A1SEC1	A1SEC0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
6-0	A1SEC[6:0]	Alarm 1 second register (BCD). When ALM1C0 = 1, second register (SEC) equal A1SEC and the other enabled alarm 1 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.50 Alarm 1 Minute Register

FFB1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1MIN	-	A1MIN6	A1MIN5	A1MIN4	A1MIN3	A1MIN2	A1MIN1	A1MIN0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	*	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
6-0	A1MIN[6:0]	Alarm 1 minute register (BCD). When ALM1C2 = 1, minute register (MIN) equal A1MIN and the other enabled alarm 1 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.51 Alarm 1 Hour Register

FFB2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1HR	-	-	A1HR5	A1HR4	A1HR3	A1HR2	A1HR1	A1HR0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	-	-	*	*	*	*	*	*
Reset Value(WDT/LVR/PIN)	-	-	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description

5-0	A1HR[5:0]	Alarm 1 hour register (BCD). When ALM1C2 = 1, hour register (HR) equal A1MIN and the other enabled alarm 1 registers meet the conditions too, generate an alarm and set the flag bit of alarm interrupt to 1.

Table 8.52 RTC calibration control register

FFB3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCCON	RTCRD	ITEN	ITS1	ITS0	OUTEN1	OUTEN0	OUTS	OUTF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	0	*	*	*	0	0	*	*
Reset Value(WDT/LVR/PIN)	0	u	u	u	0	0	u	u

Bit Number	Bit Mnemonic	Description
7	RTCRD	Time Registers Lock bit 0： RTC Time Registers update with RTC clock frequency 1： RTC Time Registers update to the latest data, then stop refresh
6	ITEN	RTC Built-in Timer Enable bit 0：Stop build-in timer 1：Start build-in timer
5-4	ITS[1:0]	RTC Build-in Timer Clock Source Select bit 00：RTC clock source / 128 01：Second (original) 10：Minute 11： Hour
3-2	OUTEN[1:0]	RTC Multi-function Output Enable bit X0：CALOUT use as normal I/O pin 10：CALOUT output RTC multi-function signal 11：CALOUT2 output RTC multi-function signal
1	OUTS	RTC Multi-function Output's Polarity Select bit 0：Positive, active level is high level 1： Negative, active level is low level
0	OUTF	Calibration Mode CALOUT Pin Output Frequency Select bit 0：Output low-frequency compensated cycles of 1s. 1：reserved

Note :
There is a delay (less than 32us) exist, when set RTCRD = 1. Because refresh the time register need time, and when RTCRD is set to 1 success, the lock operation success.
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Table 8.53 RTC Time Data Write-protect Register

FFB4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCWR	RTCWR7	RTCWR6	RTCWR5	RTCWR4	RTCWR3	RTCWR2	RTCWR1	RTCWR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	0	0	0	0	0	0	0	0
Reset Value(WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description

7-0	RTCWR[7:0]	When RTCWD = 0x69, stop the update of time registers and make this registers (include RTCPSW) writable. Then write data to time registers. At last, set RTCPSW = 0x5a, will check the data you write. When the data is under rule of each register, write success and clear RTCPSW. When the data is illegal, cancel write operation and set RTCPSW = 0x01.

Table 8.54 RTC Time Writable Register

FFB5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCPSW	PSW7	PSW6	PSW5	PSW4	PSW3	PSW2	PSW1	PSW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR)	0	0	0	0	0	0	0	0
Reset Value(WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PSW[7:0]	Set RTCPSW = 0x5a, will check the data you write. When the data is under rule of each register, write success and clear RTCPSW. When the data is illegal, cancel write operation and set RTCPSW = 0x01.

Table 8.55 RTC Interrupt Enable Register

FFB6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCIE	IT0IE	DAYIE	HRIE	MINIE	SECIE	ALM1IE	ALM0IE	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset Value(POR)	0	0	0	0	0	0	0	-
Reset Value(WDT/LVR/PIN)	0	0	0	0	0	0	0	-

Bit Number	Bit Mnemonic	Description
7	IT0IE	Build-in Timer Interrupt Enable Control bit 0: Disable build-in timer interrupt 1: Enable build-in timer interrupt
6	DAYIE	Day Interrupt Enable Control bit 0: Disable Day interrupt 1: Enable Day interrupt
5	HRIE	Hour Interrupt Enable Control bit 0: Disable Hour iInterrupt 1: Enable Hour interrupt
4	MINIE	Minute Interrupt Enable Control bit 0: Disable Minute interrupt 1: Enable Minute interrupt
3	SECIE	Second Interrupt Enable Control bit 0: Disable Second interrupt 1: Enable Second interrupt
2	ALM1IE	Alarm 1 Interrupt Enable Control bit 0: Disable Alarm 1 interrupt 1: Enable Alarm 0 interrupt
1	ALM0IE	Alarm 0 Interrupt Enable Control bit 0: Disable Alarm 0 interrupt 1: Enable Alarm 0 interrupt

Table 8.56 RTC Interrupt Request Register

FFB7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCIF	IT0IF	DAYIF	HRIF	MINIF	SECIF	ALM1IF	ALM0IF	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Reset Value(POR)	*	*	*	*	*	*	*	-
Reset Value(WDT/LVR/PIN)	u	u	u	u	u	u	u	-

Bit Number	Bit Mnemonic	Description
7	IT0IF	The Request Flag for Built-in Timer Interrupt 0: No request 1: Request
6	DAYIF	The Request Flag for Day Interrupt 0: No request 1: Request
5	HRIF	The Request Flag for Hour Interrupt 0: No request 1: Request
4	MINIF	The Request Flag for Minute Interrupt 0: No request 1: Request
3	SECIF	The Request Flag for Second Interrupt 0: No request 1: Request
2	ALM1IF	The Request Flag for Alarm 1 Interrupt 0: No request 1: Request
1	ALM0IF	The Request Flag forAlarm 0 Interrupt 0: No request 1: Request

Table 8.57 RTC Room Temperature Error Register

FFB9H-FFB8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCECH (FFB9H)	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8
RTCECL (FFB8H)	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R/W	R	R	R	R	R	R	R	R
Reset Value(POR/WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
15-0	EC[15:0]	RTC 25℃（77℉）Error Value (EC Register) E[15:0] (Two's complement) is the frequency (32768Hz) error under 25℃(77℉), 1LSB ->0.1PPM

Table 8.58 RTC Internal timerRegisters

FFBAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RTCTMR	RTCT7	RTCT6	RTCT5	RTCT4	RTCT3	RTCT2	RTCT1	RTCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	u	u	u	u	u	u	u	u

Bit Number	Bit Mnemonic	Description
7-0	RTCT[7:0]	RTC Build-in Timer Counter

NOTE:
This Counter is down-couter.1 when set RTCTMR = 0/1, overflow will be happened in every count cycle.
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8.6 Low-voltage detection (LPD1)

G80F975A is integrated with 3 LPD, and the voltage of 3 sets of power supply is tested respectively.

8.6.1 LPD1:

Low voltage detection Function (LPD1) is used to monitor VDD voltage and VIN pin voltage.VIN pin voltage detection Function is selected by the code whether its Function is valid.If VIN pin detection Function is effective, the VIN pin voltage is lower than 1.2V, and the hardware setting label FVIN is 0;If the pin voltage is higher than 1.2V, the hardware setting FVIN is marked as 1.The low voltage detection circuit detects that VDD voltage is lower than 3V, then the hardware setting tag FVDD is 0;If VDD is detected higher than 3V, the hardware setting tag FVDD is 1.

The low voltage detection Function provides the VIN pin and VDD voltage marker to the power management Function, but only the VDD voltage mark can realize automatic switching of power supply.

Table 8.87 Low-voltage detection control register

C6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON1	LPD1EN	FVIN	LPD1IF	FVDD	LPD1SF	VINITM1	VINITM0	-
R/W	R/W	R	R/W	R	R	R/W	R/W	-
Reset Value(POR/WDT/LVR/PIN)	1	0	0	0	0	0	0	-

Bit Number	Bit Mnemonic	Description
7	LPD1EN	LPD Enable bit 0: Disable lower power detection 1: Enable lower power detection
6	FVIN	VIN pin voltage status flags 0: VIN pin voltage lower than 1.2V 1: VIN pin voltage higher than 1.2V If the code choose to disable the VIN voltage detection function, this flag is invalid
5	LPD1IF	LPD interrupt flag 0: No LPD interrupt happen 1: LPD interrerupt happens
4	FVDD	Power supply status 0: battery-powered to VOUT 1: External power supply to VOUT
3	LPD1SF	VDD voltage state marker 0: VDD voltage lower than 3V 1: VDD voltage higher than 3V
2-1	VINITM[1:0]	VIN Interrupt mode selection 00：edge-triggered 01：Low level trigger (<1.2V) 1x：High level trigger (>1.2V)

8.6.2 LPD2&3:

LPD2 is used to monitor the voltage state of VOUT power supply.LPD3 is used to monitor the voltage state of VFCAP pins.

Table 8.88 VOUT(LPD2) Low-voltage detection control register

C7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON2	LPD2EN	LPD2F	LPD3EN	LPD3F	LPDS3	LPDS2	LPDS1	LPDS0
R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	1	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	LPD2EN	LPD2 Enable bit 0: Disable lower power detection 1: Enable lower power detection
6	LPD2F	LPD2 State Flag bit 0: Cleared by hardware when VOUT>LPD detect voltage. 1: Set to ‘1’ by hardware when VOUT>LPD detect voltage. Notes：When LPDEN=0, LPDF=0.
5	LPD3EN	LPD3 Enable 0: Disable lower power detection 1: Enable lower power detection（default）
4	LPD3F	VFCAP Voltage State Flag bit 0：VFCAP<3V 1：VFCAP>3V
3-0	LPDS[3:0]	LPD2 Voltage Control bits 0000: 2.55 V 0001: 2.70 V 0010: 2.85 V 0011: 3.00 V 0100: 3.15 V 0101: 3.30 V 0110: 3.45 V 0111: 3.60 V 1000: 3.75 V 1001: 3.90 V 1010: 4.05 V 1011: 4.20 V 1100: 4.35 V 1101: 4.50 V 111X: 4.65 V

8.7 Low Voltage Reset（LVR）

8.7.1 Features

LVR is about 30-60us.
An internal reset indicates low voltage reset generates

The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage is below the specified value VLVR. The LVR de-bounce Timer TLVR is about 30-60us.
The LVR circuit has the following functions when the LVR function is enabled: (t means the time of the supply voltage below VLVR)
Generates a system reset when VDD ≤ VLVR and t ≥ TLVR.
Cancels the system reset when VDD > VLVR or VDD < VLVR, but t < TLVR.
The LVR function is enabled by the Code Option.
It is typically used in AC line or large battery supplier applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage. This feature is can protect system from working under bad power supply environment.

8.8 Watchdog Timer (WDT) and reset state

8.8.1 Features

WDT runs even in the Power-Down mode

Auto detect Program Counter(PC) over range, and generate OVL Reset

Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, G80F975A built in Program Counter (PC) over range detect circuit, if program counter value is larger than flash rom size, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, user should fill unused flash rom with A5H.

WDT

The watchdog timer is a down counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled permanently by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow frequency. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

There are also some reset flags in this register as below:

8.8.2 Registers

Table 8.89 RSTSTAT Control Register

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Mnemonic	Description
7	WDOF	Watch Dog Timer Overflow or OVL Reset Flag Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows and no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	PORF	Power On Reset Flag Set only by Power On Reset, cleared only by software 0: No Power On Reset. 1: Power On Reset occurred.
4	LVRF	Low Voltage Reset Flag Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	CLRF	External Pin Reset Flag Set only by External Pin Reset, cleared by software or Power On Reset 0: No External Pin Reset occurs 1: External Pin Reset occurred
2-0	WDT[2:0]	WDT Overflow period control bit 000: Overflow period minimal value = 4096ms 001: Overflow period minimal value = 1024ms 010: Overflow period minimal value = 256ms 011: Overflow period minimal value = 128ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms Notes: If WDT_opt is enable in application, user must clear WatchDog periodically, and the interval must be less than the value list above.

8.9Power Management

G80F975A provides three kinds of power supply mode, respectively is the external power supply from the VDD input via switch to VOUT pin, external farad capacitor from VFCAP input via switch to VOUT pin, battery from VBAT pin input via switch to VOUT.

Normal power supply is provided by external power supply. If the external power supply fails, the external power supply will be automatically cut to VFCAP. If the VFCAP voltage is lower than 3V, it will automatically switch to the battery power supply.

If the external power supply is restored, the battery or VFCAP is automatically cut to the external power supply.

The external power supply voltage test is realized by the built-in low voltage detection LPD1.

The switch between the battery and the VFCAP power supply is realized by the built-in low voltage detection LPD3. When the VDD power is less than 3V, the system will be powered by VFCAP if the VFCAP is higher than 3V, otherwise it will be powered by the battery.

Switch power supply mode by the power management implemented automatic or software control, automatic switching Function can be controlled by the Registers its operation, or banned.

Whether it is the external power supply VDD alone or VFCAP alone power supply or the battery alone, or both, the power supply at the same time, G80F975A can work normally.

Automatic switching Function by AUTOS dropped (PWRCON1.0) choose to allow or prohibit, in order to ensure the right to write, and power-saving mode to enter, you must first write 55 h to the power switch control Registers, rear 1 or 0 AUTOS dropped qing (PWRCON1.0), must be continuous instruction, otherwise automatic switching Function is invalid.

If automatic switching Function is prohibited by AUTOS (pwrcon.0), power supply mode switching can also be achieved through software.

In order to ensure that it is not miswritten, in the same way as the power-saving mode, it is necessary to write 55H to the power switch to control RegistersPASLO and set the power supply, which must be ordered continuously, otherwise the power supply mode switch is invalid.

In addition, G80F979 also built load circuit in VDD pin, so as to avoid the excessive variation of VDD pin load during power switching, which resulted in large voltage fluctuation of VDD pin and frequent power switching.

The load circuit consists of a 3K resistor and a control switch. When the control switch is closed, 3K resistance is connected to the VDD pin and GND.

Control switch

VDDDISC bit control by PWRCON2.

8.9.1 Registers

Table 8.9.0 Power switching control register

E7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PASLO	PASLO.7	PASLO.6	PASLO.5	PASLO.4	PASLO.3	PASLO.2	PASLO.1	PASLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	PASLO[7:0]	This register is used to control power switching Only consecutive instructions to modify the PWRCON/LDOCON Registers control register after writing 55H to PASLO enable the power supply status and automatical power supply switching written control.，Otherwise, in the next cycle PASLO will be cleared by hardware, and AUTOS or VOUTS1:0] change back to the previous value.

Table 8.9.1 Power control register1

B3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWRCON1	-	-	-	-	-	VOUTS1	VOUTS0	AUTOS
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	-	-	-	-	-	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description

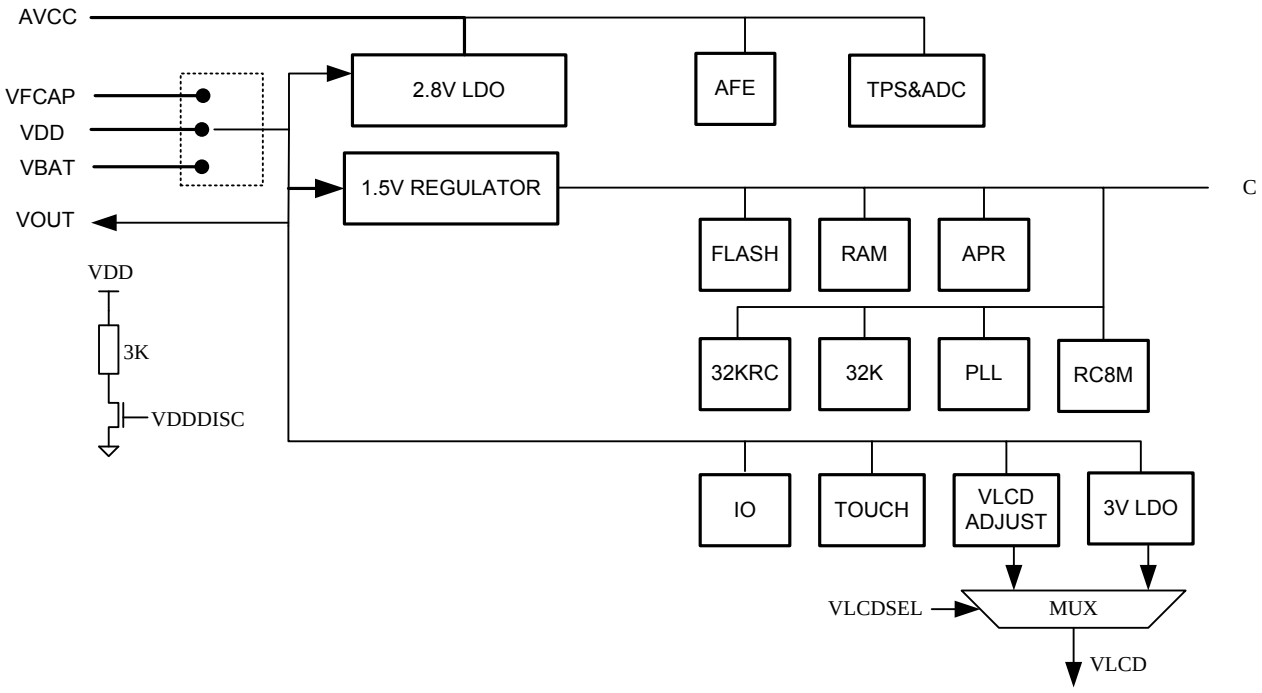
2-1	VOUTS[1:0]	State of power supply 00: VDD supply toVOUT 01: VFCAP supply to VOUT 1X: VBAT supply to VOUT
0	AUTOS	Automatic switching of power supply allows. 0：Allow automatic switching of power supply. 1：Automatic switching of power supply is forbidden.

Table 8.9.2 Power control register2

B4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWRCON2	LDO28ON	LCDLDO1	LCDLDO0	VDDDISC	-	-	-	-
R/W	R/W	R/W	R/W	R/W		-	-	-
Reset Value(POR/WDT/LVR/ PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	-	-	-	-

Bit Number	Bit Mnemonic	Description
7	LDO28ON	2.8V LDO circuit switch control. 0：close 1：open
6-5	LCDLDO[1:0]	LCDLDOVoltage regulation: 00:3V 01:2.95V 10:3.05V 11:3.1V
4	VDDDISC	VDD Load switch control 0: VDD does not receive internal 3K load. 1: VDD does receive internal 3K load.

各Function模块的供电状况如下:



8.9.2 Low-power mode

To reduce power consumption, G80F975A supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

Idle mode and super idle mode

Idle mode :In this mode, the clock to CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all be retained.

By two consecutive instructions: setting SUSLO register as 55H, and immediately followed by setting the IDL bit in PCON register, will make SH79F642B enter idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter IDLE mode.

The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

(1) An interrupt generated. After warm-up time, the clock to the CPU will be restored, and the hardware will clear SUSLO register and IDL bit in PCON register. Then the program will perform the interrupt service routine first, and then jumps to the instruction immediately following the instruction that activated Idle mode.

(2) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled), this will restore the clock to the CPU, the SUSLO register and the IDL bit in PCON register will be cleared by hardware, finally the SH79F642B will be reset. And the program will perform from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Power-Down mode

The Power-Down mode places the G80F975A in a very low power state. Power-Down mode will stop all the clocks including CPU and peripherals. If WDT is enabled, WDT block will keep on working. When entering Power-Down mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the PD bit in PCON register, will make SH79F642B enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. And the CPU will not enter Power-Down mode.

The setting of PD bit will be the last instruction that CPU performed.

Note: If IDL bit and PD bit are set simultaneously, the G80F975A enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit form Power-Down mode.

There are two ways to exit the Power-Down mode:

(1) An active external Interrupt such as INT0, INT1, INT2 ,INT3 and RTC Interrupt and Touch KEY Interrupt and LPD Interrupt will make G80F975A exit Power-Down mode. The oscillator will start after interrupt happens, after warm-up time, the clocks to the CPU and peripheral will be restored, the SUSLO register and PD bit in PCON register will be cleared by hardware. Program execution resumes with the interrupt service routine. After completion of the interrupt service routine, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) Reset signal (WDT RESET if enabled, LVR REST if enabled). This will restore the clock to the CPU after warm-up time, the SUSLO register and the PD bit in PCON register will be cleared by hardware, finally the G80F975A will be reset. And the program will perform from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

Note: In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.

Function module working status in each mode.

Mode / Function	Normal	Idle	Power-Down
Disabled Functions		CPU	CPU, EUART0 & 1 & 2& 3, TIMER0 & 1 & 2
Functions controlled by software	PLL, LCD, ADC(TPS), LPD, EUART0 & 1 & 2& 3, TIMER0 & 1 & 2, PWM,Touch KEY	Energy Metering, PLL, LCD, ADC, LPD, EUART0 & 1 & 2& 3, TIMER0 & 1 & 2, PWM, Touch KEY	Energy Metering (Constant Metering Mode),PLL, LCD, LPD, ADC(TPS), PWM ,Touch KEY
Functions controlled by Code Option	WDT, LVR	WDT, LVR	WDT, LVR
Functions always work	CPU, RTC, External Interrupt	RTC, External Interrupt	RTC, External Interrupt

In order to further reduce the power consumption of power down mode, can reduce the power down mode by temporarily 1.55 V voltage regulator to reduce power consumption, the normal work of the regualtor voltage is not controlled by the Registers, when 1.55 V voltage regulator can be set through the following Registers:

Table 8.93 LDO Control Register:

B5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDOCON	LPEN3	LPEN2	LPEN1	LPEN0	-	LDOVOL2	LDOVOL1	LDOVOL0
R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	-	1 u 1 1	0 u 0 0	1 u 1 1

Bit Number	Bit Mnemonic	Description
7-4	LPEN[3:0]	LDO Low Function enable Registers： When the LPEN[3:0]=0x5, the current RegistersLDOVOL[2:0] is used to set the set value as 1.55v regulator voltage, and the other values close the Function.
2-0	LDOVOL[2:0]	1.5V regulator LDO Voltage Registers Regulation: 000:1.30V 001:1.35V 010:1.40V 011:1.45V 100:1.50V 101:1.55V (default) 110:1.60V 111:1.65V Note: it must be LDOLO=0X55, and LDOCON is allowed to write operations.

The Registers only x55 PASLO = 0, can be modified

Table 8.94 Power control register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	SSTAT1	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/ PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	SMOD	Baudrate Speed-up bit of EUART
6	SSTAT	SCON[7:5] Function Selector
5	SSTAT1	SCON1[7:5] Function Selector
3-2	GF[1:0]	SCON2[7:5] Function Selector
1	PD	General-purpose flag for software
0	IDL	Power-Down Mode control bit 0: Cleared by hardware when an interrupt or reset occurs. 1: Set by software to activate the Power-Down mode.

Table 8.95 Suspend Mode Control register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value(POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	SUSLO[7:0]	This register is used to control the CPU enter suspend mode (IDLE or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle

Program example:

```
IDLE_MODE:
MOV     SUSLO, #55H
ORL     PCON, #01H
NOP
NOP
NOP
```

```
POWERDOWN_MODE:
MOV     SUSLO, #55H
ORL     PCON, #02H
NOP
NOP
NOP
```

8.10 Warm-up Timer

8.10.1 Features

Built-in power on warm-up counter to eliminate unstable state of power on

Built-in oscillator warm-up counter to eliminate unstable state when oscillation startup

G80F975A has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read customer option etc.

G80F975A has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from Power-down mode.

After power-on, G80F975A will start power warm-up procedure first, and then oscillator warm-up procedure.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		WDT Reset (Not in Power-Down Mode)		WDT Reset (Wakeup from Power-Down Mode)		Wakeup from Power-Down Mode (Only for interrupt)	
TPWRT	OSC Warm up Time	TPWRT	OSC Warm up Time	TPWRT	OSC Warm up Time	TPWRT	Power on oscillator Preheating counting time
11ms	YES	1000CKs	None	11ms	YES	1000CKs	Low frequency 1 High frequency has

Oscillator Warm-up Time Table

Oscillator type	Warm-up time
32.768kHz crystal	213 X Tosc
8MHz RC crystal	27 X THRC
32kHz RC crystal	27 X TLRC

CKS：Internal RC：2MHz

8.11 Code option

OP_WDT：
0: disable watchdog (WDT) fuction（default）
1: enable watchdog (WDT) fuction

OP_WDTPD：
0: disable watchdog fuction in Power-down mode
1: enable watchdog fuction in Power-down mode
OP_WDTIDL：
0: disable watchdog fuction in Super-IDLE mode（default）
1:enable watchdog fuction in Super-IDLE mode
OP_LVREN：
0: disable Low Voltage Reset (LVR) fuction（default）
1: enable Low Voltage Reset (LVR) fuction
OP_RST：
0：P1.0 as RST pin（default）
1：P1.0 as I/O pin
OP_VIN：
0： P0.3 as VIN pin
1： P0.3 as I/O pin（default）
OP_EEPROMSIZE:
1111: 8 x 512Bytes
1110: 7 x 512Bytes
1101: 6 x 512Bytes
1100: 5 x 512Bytes
1011: 4 x 512Bytes
1010: 3 x 512Bytes
1001: 2 x 512Bytes
1000: 1 x 512Bytes
other: 0 bytes（default）

9.Energy Metering

9.1 Features

G80F975A provides all the features that single-phase energy metering needed, including active power and active energy, reactive power and reactive power, apparent power and apparent energy, voltage/ current RMS and frequency calculation to support flexible anti-tampering program and calibration program.
Active energy error less than 0.1% in the dynamic range of 3000:1
Active energy error less than 0.1% in the dynamic range of 1500:1
Voltage/ Current RMS , Voltage frequency measurement.
Pulse output PF/QF
Zero-corss and voltage sag interrupt detection
Supporting dc metering
Support the zero-line metering mode, and the power consumption is low to 800 uA when the 3-way ADC is measured.
support DIMMER power detection
support rapid current
support constant measurement model
Supports software control pulse output
Supports single phase, 3 wire service
small current acceleration correction table
G80F975Aenergy metering unit (EMU) is composed of the analog front-end (AFE) and digital signal processor (DSP). The analog front-end acquisition two current signal and one voltage signal, the digital signal processor to complete the metering function of the active power and active energy, reactive power and reactive energy, voltage rms, current rms and frequency calculation. By the SFR registers and interrupt mode, the digital signal processing part can config calibration parameters and read metering parameters.The PF/QF pin output the result of metering (Calibration pulse output) can be connected directly to the standard meter to contrast error. EMU clock isselectable.

9.2 Analog Front End（AFE）

G80F975A analog front end includes three analog gain amplifier (PGA), three Σ-Δ analog-to-digital converter (ADC) and a reference voltage (VREF). The analog front end collects and quantifies the voltage and current signal.

9.2.1 Analog Gain Amplifie r（PGA）

The analog gain amplifier completes to amplify the amplitude of the input differential signal, then the signal be sent to ADC after the multiplexer to ensure the linearity of the measurement when the minimal signal input. The magnification of 1,2,4,8,16 of the three PGA can be configured independently through the register.

	magnification	Maximum input signal
Voltage circuit	2	0.2V
	4	0.1V
Current path	2	0.2V
	4	0.1V
	8	0.05V
	16	0.025V

9.2.2 Analog-to-Digital Converter（ADC）

G80F975A have 23 bits sigma-delta ADC, quantized voltage and current input.
The indirect register I1DTA, I2DTA and VDTA store two-channel current and one channel voltage ADC output value,and update frequency is 19.2MHz

9.2.3 Reference Voltage（VREF）

ADC embedded high precision bandgap reference voltage, the ADC voltage reference. Voltage value of 1.4V, the temperature coefficient of ± 25ppm / ℃

9.3 Digital Signal Processor（DSP）

Digital signal processor accept the voltage and current quantized value of FIR output, and implement the digital signal processing, to get the energy data such as active energy, reactive power, voltage and current rms and output pulse of active and reactive power.

9.4 Registers

EMU, including two types of registers, one is SFR registers, the direct register, accessed by SFR address directly; the other is metering parameters and calibration parameter register, indirect register, indirectly accessed by direct register

9.4.1 SFRRegisters

EMU SFR Registers

Addresss	Name	Description
91H	EADR	EMU Address Register
92H	EDTAH	EMU High Byte Data Register
93H	EDTAM	EMU Mid Byte Data Register
94H	EDTAL	EMU Low Byte Data Register
95H	EMUSR	EMU Status/ Control Register
96H	EMUIE	EMU Interrupt Enable Register
97H	EMUIF	EMU Interrupt Flag Register

Table 9.1 EMU Address Register

91H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EADR	RW	EADR.6	EADR.5	EADR.4	EADR.3	EADR.2	EADR.1	EADR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	RW	EMU Indirect RegisterRead/ Write Flag 0：Read EMU indirect register 1：Write EMU indirect register
6-0	EADR[6:0]	EMU Address Register

Table 9.2 EMU High Byte Register

92H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EDTAH	EDTAH.7	EDTAH.6	EDTAH.5	EDTAH.4	EDTAH.3	EDTAH.2	EDTAH.1	EDTAH.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	EDTAH[7:0]	EMU High Byte Data Register

Table 9.3 EMU Mid Byte Register

93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EDTAM	EDTAM.7	EDTAM.6	EDTAM.5	EDTAM.4	EDTAM.3	EDTAM.2	EDTAM.1	EDTAM.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	EDTAM[7:0]	EMU Mid Byte Data Register

Table 9.4 EMU Low Byte Register

94H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EDTAL	EDTAL.7	EDTAL.6	EDTAL.5	EDTAL.4	EDTAL.3	EDTAL.2	EDTAL.1	EDTAL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	EDTAL[7:0]	EMU Low Byte Register

Table 9.5 EMU Status/ Control Register

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUSR	DSPEN	EMUCLKS1	EMUCLKS0	SAGF	NoQLd	NoPLd	REVQ	REVP
R/W	R/W	R/W	R/W	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
7	DSPEN	DSP Gate 0：Disable 1：enable
6-5	EMUCLKS[1:0]	EMU Clock Select 00：Close the EMU clock input. 01：Select the 32K clock as the EMU module working clock. 10：Select and enable the RC8M clock to work as the EMU module working clock. 11：Select and enable the PLL clock to work as the EMU module working clock.
4	SAGF	Loss of pressure status symbol. 0：normal state 1：unnormal state
3	NoQLd	Reactive Power no load Flag 0：Reactive power is greater than or equal to the startup power 1：Reactive power is less than the startup power
2	NoPLd	Active Power no load Flag 0：Active power is greater than or equal to the startup power 1：Active power is less than the startup power
1	REVQ	Reverse Reactive Energy Flag 0：Positive reactive energy 1：Negative reactive energy
0	REVP	Reverse Active Energy Flag 0：Positive active energy 1：Negative active energy

NOTE:

When DSPEN = 0, clear power and RMS's calculate register, except the parameters configuration and energy accumulation register.

9.4.2 Indirect Register

The indirect registers include metering parameter registers and calibration parameter registers

All metering parameter registers are read-only but FREQ which can only be read by the EADR EDTAH / EDTAM / EDTAL register indirect

1. EDTAH / EDTAM / EDTAL are stored 3 bytes of high, mid, low byte data if the metering parameter register is a 3-byte register.
2. EDTAM / EDTAL are stored 2 bytes of mid, low byte data, and EDTAH is sign-extension bit of EDTM.7, if the metering parameter register is a 2-byte register

Operating rules of metering parameters: first,write the accessed register address to EADR, read/ write flag is 0, then the metering data of corresponding address update to the SFR registers EDTAH / EDTAM / EDTAL,finally, access EDTAH / EDTAM / EDTAL register

1. EDTAM and EDTAL are high and low bytes data of calibration parameter configuration register, if the parameter configuration register is a 2-byte register.
2. EDTAL is the data of calibration parameter configuration register and EDTAM data is invalid, if the parameter configuration register is a single-byte register.

Operating rules of calibration parameters

1. To access parameter configuration registers, first, write the accessed register address to EADR, read/ write flag is 0, then the calibration parameter data of corresponding address update to the SFR registers EDTAM / EDTAL, finally, access EDTAM / EDTAL register.
2. To write the calibration parameter configuration registers, first, write data to EDTAM / EDTAL, then, write the accessed register address to EADR, read/ write flag is 1, then, the data of EDTAM / EDTAL registers update to calibration parameter configuration registers of corresponding address.

Note: As the internal of EMU indirect register using a separate mechanism to read and writ, except this order, several NOP need to be inserted after the EADR register read and write commands, then operate EDATH, EDATM, EDATL, more than 3 NOP need to be inserted when the system clock is 9.8304MHz.

Metering Parameter Register

EMU Metering Parameter Register list

addr	Name	bytes	Description
00H	I1DTA	3	ADC output value of current channel 1
01H	I2DTA	3	ADC output value of current channel 2
02H	VDTA	3	ADC output value of voltage channel
03H	APWR1H	3	Channel 1 instantaneous active power value register high
04H	RPWR1H	3	Channel 1 instantaneous reactive power value register high
05H	APWR2H	3	Channel 2 instantaneous active power value register high
06H	RPWR2H	3	Channel 2 instantaneous reactive power value register high
07H	AERY	3	Active energy value
08H	RERY	3	Reactive energy value
09H	FREQ	2	Voltage frequency value
0AH	I1Rms	3	Current rms of channel 1
0BH	I2Rms	3	Current rms of channel 2
0CH	VRMS	3	Voltage rms
0DH	WPA	3	Active energy pulse accumulated value
0EH	VARPA	3	Reactive energy pulse accumulated value
0FH	APWRA1H	3	Active power average value of channel 1 register high
10H	RPWRA1H	3	Reactive power average value of channel 1 register high
11H	APWRA2H	3	Active power average value of channel 2 register high
12H	RPWRA2H	3	Reactive power average value of channel 2 register high
13H	AERYL	3	Active energy low value
14H	RERYL	3	Reactive energy low value
15H	VDTAMAX	3	MAX ADC sampling value of voltage channel
16H	AERY_CONSTH	3	Constant mode active power cumulative value
17H	RERY_CONSTH	3	Constant mode reactive power cumulative value
18H	AERY_CONSTL	3	Constant mode active power cumulative value register low
19H	RERY_CONSTL	3	Constant mode reactive power cumulative value register low

1AH	WPA_CONST	3	Constant mode active energy pulse accumulated value
1BH	VARPA_CONST	3	Constant mode reactive energy pulse accumulated value
20H	APWRA1L	2	average active power value of Channel 1 register low (CmodeFreq[2]=0)
21H	RPWRA1L	2	average reactive power value of Channel 1 register low (CmodeFreq[2]=0)
22H	APWRA2L	2	average active power value of Channel 2 register low (CmodeFreq[2]=0)
23H	RPWRA2L	2	average reactive power value of Channel 2 register low (CmodeFreq[2]=0)
24H	APWR1L	2	Active power value channel 1 register low
25H	RPWR1L	2	Reactive power value channel 1 register low
26H	APWR2L	2	Active power value channel 2 register low
27H	RPWR2L	2	Reactive power value channel 2 register low

Table 9.6 ADC output value of current channel 1

00H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
I1DTA	I1DTA.23	I1DTA.22	I1DTA.21	I1DTA.20…3	I1DTA.2	I1DTA.1	I1DTA.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	I1DTA[23:0]	ADC output value of current channel 1, the binary complement means a signed value

Table 9.7 ADC output value of current channel 2

01H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
I2DTA	I2DTA.23	I2DTA.22	I2DTA.21	I2DTA.20…3	I2DTA.2	I2DTA.1	I2DTA.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	I2DTA[23:0]	ADC output value of current channel 2, the binary complement means a signed value

Table 9.8 ADC output value of voltage channel

02H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VDTA	VDTA.23	VDTA.22	VDTA.21	VDTA.20…3	VDTA.2	VDTA.1	VDTA.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VDTA[23:0]	ADC output value of voltage channel, the binary complement means a signed value

Table 9.9 Channel 1 instantaneous active power value register high

03H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
APWR1H	APWR1H.23	APWR1H.22	APWR1H.21	APWR1H.20…3	APWR1H.2	APWR1H.1	APWR1H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	APWR1H[23:0]	Channel 1 instantaneous active power value register high, the binary complement means a signed value

Table 9.10 Channel 1 instantaneous reactive power value register high

04H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RPWR1H	RPWR1H.23	RPWR1H.22	RPWR1H.21	RPWR1H.20	RPWR1H.2	RPWR1H.1	RPWR1H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPWR1H[23:0]	Channel 1 instantaneous reactive power value register high，the binary complement means a signed value

Table 9.11 Channel 2 instantaneous active power value register high

05H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
APWR2H	APWR2H.23	APWR2H.22	APWR2H.21	APWR2H.20	APWR2H.2	APWR2H.1	APWR2H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	APWR2H[23:0]	Channel 1 instantaneous active power value register high .the binary complement means a signed value

Table 9.12 Channel 2 instantaneous reactive power value register high

06H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RPWR2H	RPWR2H.23	RPWR2H.22	RPWR2H.21	RPWR2H.20	RPWR2H.2	RPWR2H.1	RPWR2H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPWR2H[23:0]	Channel 2 instantaneous active power value register high .the binary complement means a signed value

Table 9.13 active energy value（CONST_EN=0）

07H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
AERY	AERY.23	AERY.22	AERY.21	AERY.20…3	AERY.2	AERY.1	AERY.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERY[23:0]	active energy value，the binary complement means a signed value

Table 9.14 Reactive energy value（CONST_EN=0）

08H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RERY	RERY.23	RERY.22	RERY.21	RERY.20…3	RERY.2	RERY.1	RERY.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY[23:0]	Reactive energy value. the binary complement means a signed value

Table 9.15 Voltage frequency value

09H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
FREQ	FREQ.15	FREQ.14	FREQ.13	FREQ.12…3	FREQ.2	FREQ.1	FREQ.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	FREQ[15:0]	Voltage frequency value, unsigned value, reset value 00H

The frequency value is a 16 bit unsigned number, The frequency value is obtained by counting the voltage channel 2 times forward zero, and the update cycle is twice as long as the input signal period, and the measurement range is 40~70Hz.
The conversion formula of frequency is：ADCCKSEL/FREQ

Table 9.16 Current rms of channel 1

0AH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
I1Rms	I1Rms.23	I1Rms.22	I1Rms.21	I1Rms.20…3	I1Rms.2	I1Rms.1	I1Rms.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	I1Rms[23:0]	Current rms of channel 1, , unsigned value

Table 9.17 Current rms of channel 2

0BH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
I2Rms	I2Rms.23	I2Rms.22	I2Rms.21	I2Rms.20…3	I2Rms.2	I2Rms.1	I2Rms.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	I2Rms[23:0]	Current rms of channel 2, unsigned value

Table 9.18 Voltage rms

0CH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VRMS	VRMS.23	VRMS.22	VRMS.21	VRMS.20…3	VRMS.2	VRMS.1	VRMS.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VRMS[23:0]	Voltage rms, unsigned value

Voltage/ current rms update frequence is set by SUMSAMPS register.

Table 9.19 Active energy pulse accumulated value（CONST_EN=0）

0DH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
WPA	WPA.23	WPA.22	WPA.21	WPA.20…3	WPA.2	WPA.1	WPA.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	WPA[23:0]	Active energy pulse accumulated value，unsigned value

Table 9.20 Reactive energy pulse accumulated value（CONST_EN=0）

0EH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VARPA	VARPA.23	VARPA.22	VARPA.21	VARPA.20…	VARPA.2	VARPA.1	VARPA.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VARPA[23:0]	Reactive energy pulse accumulated value，unsigned value

Table 9.21 Active power average value of channel 1 register high (CmodeFreq[2]=0)

0FH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
APWRA1H	APWRA1H.23	APWRA1H.22	APWRA1H.21	APWRA1H.20	APWRA1H.2	APWRA1H.1	APWRA1H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	APWRA1H[23:0]	Active power average value of channel 1 register high，the binary complement means a signed value，the cycle of measurement is set by SUMSAMPS.

Table 9.22 Reactive power average value of channel 1 register high (CmodeFreq[2]=0)

10H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RPWRA1H	RPWRA1H.23	RPWRA1H.22	RPWRA1H.21	RPWRA1H.20	RPWRA1H.2	RPWRA1H.1	RPWRA1H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/ PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPWRA1H[23:0]	Reactive power average value of channel 1 register high (CmodeFreq[2]=0)，the binary complement means a signed value，the cycle of measurement is set by SUMSAMPS.

Table 9.23 Active power average value of channel 2 register high (CmodeFreq[2]=0)

11H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
APWRA2H	APWRA2H.23	APWRA2H.22	APWRA2H.21	APWRA2H.20	APWRA2H.2	APWRA2H.1	APWRA2H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/ PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	APWRA2H[23:0]	Active power average value of channel 2 register high，the binary complement means a signed value，the cycle of measurement is set by SUMSAMPS.

Table 9.24 Reactive power average value of channel 2 register high (CmodeFreq[2]=0)

12H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RPWRA2H	RPWRA2H.23	RPWRA2H.22	RPWRA2H.21	RPWRA2.H.2	RPWRA2H.2	RPWRA2H.1	RPWRA2H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/ PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPWRA2H[23:0]	Reactive power average value of channel 2 register high ,the binary complement means a signed value，the cycle of measurement is set by SUMSAMPS.

Table 9.25 Active energy low value（CONST_EN=0）

13H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
AERYL	AERYL.23	AERYL.22	AERYL.21	AERYL.20…3	AERYL.2	AERYL.1	AERYL.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERYL[23:0]	Active energy low value，low 24 bit.

Table 9.26 Reactive energy low value（CONST_EN=0）

14H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RERYL	RERYL.23	RERYL.22	RERYL.21	RERYL.20…3	RERYL.2	RERYL.1	RERYL.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERYL[23:0]	Reactive energy low value，low 24 bit.

Table 9.27 MAX ADC sampling value of voltage channel

15H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VDTAMAX	VDMAX.23	VDMAX.22	VDMAX.21	VDMAX.20…3	VDMAX.2	VDMAX.1	VDMAX.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VDMAX[23:0]	SUMSAMPS sets the maximum value of VDAT in the voltage sampling waveform within the cycle，a signed value

Table 9.28 Constant mode active power cumulative value

16H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
AERY_CONSTH	AERY_CONSTH.23	AERY_CONSTH.22	AERY_CONSTH.21	AERY_CONSTH.20…3	AERY_CONSTH.2	AERY_CONSTH.1	AERY_CONSTH.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERY_CONSTH[23:0]	Constant mode active power cumulative value，the binary complement means a signed value

Table 9.29 Constant mode reactive power cumulative value

17H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RERY_CONSTH	RERY_CONSTH.23	RERY_CONSTH.22	RERY_CONSTH.21	RERY_CONSTH.20…3	RERY_CONSTH.2	RERY_CONSTH.1	RERY_CONSTH.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY_CONSTH [23:0]	Constant mode reactive power cumulative value，the binary complement means a signed value

Table 9.30 Constant mode active power cumulative value register low

18H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
AERY_CONSTL	AERY_CONSTL.23	AERY_CONSTL.22	AERY_CONSTL.21	AERY_CONSTL.20…3	AERY_CONSTL.2	AERY_CONSTL.1	AERY_CONSTL.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERY_CONSTL [23:0]	Constant mode active power cumulative value register low,the binary complement means a signed value

Table 9.31 Constant mode reactive power cumulative value register low

19H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RERY_CONSTL	RERY_CONSTL.23	RERY_CONSTL.22	RERY_CONSTL.21	RERY_CONSTL.20…3	RERY_CONSTL.2	RERY_CONSTL.1	RERY_CONSTL.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY_CONSTL [23:0]	Constant mode reactive power cumulative value register low，the binary complement means a signed value

Table 9.32 Constant mode active energy pulse accumulated value

1AH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
WPA_CONST	WPA_CONST.23	WPA_CONST.22	WPA_CONST.21	WPA_CONST.20…3	WPA_CONST.2	WPA_CONST.1	WPA_CONST.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	WPA_CONST [23:0]	Constant mode active energy pulse accumulated value，unsigned value

Table 9.33 Constant mode reactive energy pulse accumulated value

1BH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VARPA_CONST	VARPA_CONST.23	VARPA_CONST.22	VARPA_CONST.21	VARPA_CONST.20…3	VARPA_CONST.2	VARPA_CONST.1	VARPA_CONST.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VARPA_CONST [23:0]	Constant mode reactive energy pulse accumulated value，unsigned value

Table 9.37 Low average reactive power value of channel 2（(CmodeFreq[2]=0)

23H	**Bit15**	**Bit14**	**Bit13**	**第12-3位**	Bit2	Bit1	Bit0
APWRA1L	RPWRA2L.15	RPWRA2L.14	RPWRA2L.13	RPWRA2L.12…3	RPWRA2L.2	RPWRA2L.1	RPWRA2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	APWRA2L[15:0]	average active power value of Channel 1 register low（(CmodeFreq[2]=0)

Table 9.38 average active power value of Channel 1 register low（(CmodeFreq[2]=0)

20H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
APWRA1L	APWRA1L.15	APWRA1L.14	APWRA1L.13	APWRA1L.12…3	APWRA1L.2	APWRA1L.1	APWRA1L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description

15-0	APWRA1L[15:0]	average active power value of Channel 1 register low（(CmodeFreq[2]=0)

Table 9.39 average reactive power value of Channel 1 register low（(CmodeFreq[2]=0)

21H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
RPWRA1L	RPWRA1L.15	RPWRA1L.14	RPWRA1L.13	RPWRA1L .12…3	RPWRA1L.2	RPWRA1L.1	RPWRA1L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	RPWRA1L[15:0]	average reactive power value of Channel 1 register low（(CmodeFreq[2]=0)

Table 9.40 average active power value of Channel 2 register low（(CmodeFreq[2]=0)

22H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
APWRA2L	APWRA2L.15	APWRA2L.14	APWRA2L.13	APWRA2L.12…3	APWRA2L.2	APWRA2L.1	APWRA2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	APWRA2L[15:0]	average active power value of Channel 2 register low（(CmodeFreq[2]=0)

Table 9.41 verage reactive power value of Channel 2 register low（(CmodeFreq[2]=0)

23H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
RPWRA2L	RPWRA2L.15	RPWRA2L.14	RPWRA2L.13	RPWRA2L .12…3	RPWRA2L.2	RPWRA2L.1	RPWRA2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	RPWRA2L[15:0]	verage reactive power value of Channel 2 register low（(CmodeFreq[2]=0)

Table 9.42 Active power value channel 1 register low

24H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
APWR1L	APWR1L.15	APWR1L.14	APWR1L.13	APWR1L.12…3	APWR1L.2	APWR1L.1	APWR1L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description

15-0	APWR1L[15:0]	Active power value channel 1 register low

Table 9.43 Reactive power value channel 1 register low

25H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
RPWR1L	RPWR1L.15	RPWR1L.14	RPWR1L.13	RPWR1L.12…3	RPWR1L.2	RPWR1L.1	RPWR1L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPWR1L[15:0]	Reactive power value channel 1 register low

Table 9.44 Active power value channel 2 register low

26H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
APWR2L	APWR2L.15	APWR2L.14	APWR2L.13	APWR2L.12…3	APWR2L.2	APWR2L.1	APWR2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	APWR2L[15:0]	Active power value channel 2 register low

Table 9.45 Reactive power value channel 2 register low

27H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
RPWR2L	RPWR2L.15	RPWR2L.14	RPWR2L.13	RPWR2L.12…3	RPWR2L.2	RPWR2L.1	RPWR2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPWR2L[15:0]	Reactive power value channel 2 register low

Calibration Parameter Register

EMU calibration parameter register list

Addresss	Name	Length	Description
30H	EMUCFG0	2	EMU configuration parameter register 0
31H	EMUCFG1	3	EMU configuration parameter register 1
32H	EMUCFG2	3	EMU configuration parameter register 2
33H	EMUCFG3	2	EMU configuration parameter register 3
34H	W1GAIN	2	Active power gain of channel 1 (active & reactive)
35H	P1CAL	2	Current phase compensation of channel 1
36H	W2GAIN	2	Active power gain of channel 2 (active & reactive)
37H	P2CAL	2	Current phase compensation of channel 2
38H	I2GAIN	2	Current gain of channel 2
39H	WATT1OS	3	Active power offset of Channel 1
3AH	WATT2OS	3	Active power offset of Channel 2
3BH	VAR1OS	3	Reactive power offset of Channel 1
3CH	VAR2OS	3	Reactive power offset of Channel 2
3DH	IRMS1OS	3	Current RMS offset of Channel 1
3EH	IRMS2OS	3	Current RMS offset of Channel 2
3FH	VRMSOS	3	Voltage RMS offset
40H	ADCOSI1	2	ADC offset of current channel 1
41H	ADCOSI2	2	ADC offset of current channel 2
42H	ADCOSU	2	ADC offset of voltage channel
43H	SPTSP	2	Active power startup settings Registers
44H	SPTSQ	2	Reactive power startup settings Registers
45H	VCONST	3	Voltage constant
46H	SAGTHR	2	Threshold configuration for voltage sag
47H	SAGCNT	2	Sampling count for voltage sag
48H	ICONT	2	Configuration for output pulse frequency
49H	PCNT	2	Fast active pulse counting, the binary complement means a signed value (CmodeFreq[2]=0).
4AH	QCNT	2	Fast reactive pulse counting, the binary complement means a signed value (CmodeFreq[2]=0).
4BH	SUMSAMPS	2	Calculate cycle
4CH	APCONST	3	Active power const
4DH	RPCONST	3	Reactive power const
4EH	PCNT_CONST	2	Fast active pulse couner, the binary complement means a signed value (CmodeFreq[2]=1).
4FH	QCNT_CONST	2	Fast reactive pulse counter, the binary complement means a signed value (CmodeFreq[2]=1).
50H	DIMTHR	3	DIMMER Determine threshold Settings.
51H	DIMCNT	1	DIMMER Differential count threshold.
52H	SAMPCON	1	Waveform sampling Configuration Registers:

5AH	HPFEFFB	3	High Pass coefficient B
5BH	HPFEFFA	3	High Pass coefficient A
60H	LPFEFFB	3	Low Pass coefficient B
61H	LPFEFFA	3	Low Pass coefficient A
62H	ULPCTRL	2	Ultra-low power Settings (control DIMMER and reactive power)
70H	AERY1H	3	Channel 1 high cumulative value of active power
71H	RERY1H	3	Channel 1 has a high cumulative value of reactive power
72H	AERY1M	3	Channel 1 median cumulative value of active power
73H	RERY1M	3	Median value of cumulative value of channel 1 reactive power
74H	AERY1L	2	Channel 1 low cumulative value of active power
75H	RERY1L	2	Channel 1 low cumulative value of reactive power
76H	AERY2H	3	Channel 2 high cumulative value of active power
77H	RERY2H	3	Channel 2 has a high cumulative value of reactive power
78H	AERY2M	3	Channel 2 median cumulative value of active power
79H	RERY2M	3	Median value of cumulative value of channel 2 reactive power
7AH	AERY2L	2	Channel 2 low cumulative value of active power
7BH	RERY2L	2	Channel 2 low cumulative value of reactive power
7CH	ICONT1	2	Second output pulse frequency setting
7DH	EMUCFG4	2	EMU metering configuration register 4

Table 9.44 EMU configuration parameter register 0

30H	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EMUCFG0				ADCCKSEL1	ADCCKSEL0			
R/W	-	-	-	R/W	R/W	-	-	-
Reset Value（POR/WDT/LVR/PIN）	-	-	-	0 u 0 0	0 u 0 0	-	-	-
30H	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
EMUCFG0								APGAU0
R/W	-	-	-	-	-	-	-	R/W
Reset Value（POR/WDT/LVR/PIN）	-	-	-	-	-	-	-	0 u 0 0
30H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUCFG0	APGAI21	APGAI20	APGAI11	APGAI10	INPUTSHORT	ADCUON	ADCI2ON	ADCI1ON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/PIN）	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
20-19	ADCCKSEL[1:0]	ADC work clock frequency division selection. EMUCLKS=01： 32K EMUCLKS=1X： 00: PLL/4=2457600, High precision mode 01: PLL/8=1228800, reserve 10: PLL/32=307200, Zero-line mode 11: PLL/64=153600, Dc measurement
8	APGAU0	Gain of analog PGA of voltage channel 0 0: 2X gain (Default) 1: 2X gain
7-6	APGAI2[1:0]	Gain of analog PGA of current channel 2 00: 2 X gain (Default) 01: 4 X gain 10: 8 X gain 11: 16 X gain
5-4	APGAI1[1:0]	Gain of analog PGA of current channel 1 00: 2 X gain (Default) 01: 4 X gain 10: 8 X gain 11: 16 X gain
3	INPUTSHORT	The channel input pins are short within the pin.
2	ADCUON	ADC enable control of channel current 0: Stop ADC(Default) 1: Start ADC
1	ADCI2ON	ADC enable control of channel current 2 0: Stop ADC(Default) 1: Start ADC
0	ADCI1ON	ADC enable control of channel current 1 0: Stop ADC(Default) 1: Start ADC

Bit Number	Bit Mnemonic	Description
15-0	EMUCFG0[15-0]	EMU Configuration of measurement Registers0，Typical configuration is 0x000067。

Table 9.45 EMU configuration parameter register 1:

31H	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EMUCFG1	POL	QFEN	PFEN	MNL	DCCON1	DCCON0	HPFON	PWidth1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT /LVR/PIN）	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0
31H	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
EMUCFG1	PWidth0	PFAST1	PFAST0	QMOD1	QMOD0	PMOD1	PMOD0	RMSLPFENB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT /LVR/PIN）	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0
31H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUCFG1	QRUN	PRUN	PWRSEL1	PWRSEL0	CONST_EN	CmodeFreq1	CmodeFreq0	Cmodeen
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT /LVR/PIN）	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23	POL	PF/QFOutput polarity control 0: High level (default) 1: Low level
22	QFEN	Reactive pulse QF pin output control. 0：No reactive pulse QF pin output is prohibited. 1：Allow reactive pulse QF pin output.
21	PFEN	Active pulse PF pin output control. 0：Power pulse PF pin output is prohibited. 1：Enable active pulse PF pin output.
20	MNL	Off Neutral Wire Mode enable mode 0: Disable Off Neutral Wire Mode (init) 1: Enable Off Neutral Wire Mode. Use the value in VCONST register (instead of ADC sampling value of voltage channel) to calculate active/reactive power value.
19-18	DCCON[1:0]	Dc metering control 0X: Turn off dc metering mode. 10: The dc metering mode is opened, and the cut-off frequency of CIC filter is 50HZ. 11: The dc metering mode is opened, and the cut-off frequency of CIC filter is 60HZ
17	HPFON	High-pass filter select of channel current 0:Open High-pass filter 1: Close High-pass filter
16-15	PWidth[1:0]	Output pulse width (be care of the effect of clock switch) 00: 90ms(+/-5%)(init) 01: 45ms(+/-5%) 10: reserve 11: 11ms(+/-5%)

14-13	PFAST[1:0]	Small-signal pulse speed up 00: 1X 01: 4X 10: 8X 11: 16X
12-11	QMOD[1:0]	Reactive Power Accumulation Method 00: Driect accumulate 01: Accumulate the positive only 10: Accumulate the absolute value 11: Driect accumulate
10-9	PMOD[1:0]	Active power accumulation method 00: Driect accumulate 01: Accumulate the positive only 10: Accumulate the absolute value 11: Driect accumulate
8	RMSLPFENB	Valid value data can be obtained through low pass. 0：The valid value data passes through the low pass (default) 1：Valid value data does not pass low.
7	QRUN	Reactive Energy Accumulation Enable 0: Disable 1: Enable
6	PRUN	Active Energy Accumulation Enable 0: Disable 1: Enable
5-4	PWRSEL[1:0]	Metering Source Channel Select 00: Channel1 01: Channel 2 10: Sum of channel 1 & 2 11: Sum of absolute value of channel 1 & 2
3	CONST_EN	Constant metering mode control. 0: Constant metering mode closed (default) 1: The constant metering mode opens.
2-1	CmodeFreq[1:0]	Cumulative frequency selection. CONST_EN=0: Fixed to update frequency *4. CONST_EN=1: For a 32768 For example,： CONST_EN=0 EMUCLKS[1:0]=11（PLL） ADCCKSEL[1:0]=00/01：The fixed update frequency is. 19.2*4 ADCCKSEL[1:0]=10：The fixed update frequency is. 4.8*4
0	Cmodeen	Accumulation Module Enable 0:Disable (init) 1: Enable

Bit Number	Bit Mnemonic	Description
23-0	EMUCFG1[23-0]	EMU calibration parameter register 1，Typical value is 0x2000C1

Table 9.46 EMU configuration parameter register 2:

32H	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
EMUCFG2	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-
Reset Value（POR/WDT/LVR/PIN）	-	-	-	-	-	-	-	-
32H	Bit15	Bit14	Bit13	Bit12	Bit10	Bit10	Bit9	Bit8
EMUCFG2	-	ADCRST_U	ADCRST_I2	ADCRST_I1	VREF_CURS.1	VREF_CURS.0	PGA_CURS.4	PGA_CURS.3

R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/PIN）	-	0 u 0 0	0 u 0 0	0 u 0 0	1 u 1 1	1 u 1 1	0 u 0 0	0 u 0 0
31H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUCFG2	PGA_CURS.2	PGA_CURS.1	PGA_CURS.0	ADC_CURS.4	ADC_CURS.3	ADC_CURS.2	ADC_CURS.1	ADC_CURS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/PIN）	1 u 1 1	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	1 u 1 1	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
14	ADCRST_U	Voltage channel analog ADC reset control. 0: ADC is in normal working condition (default) 1: The ADC is in a reset state.
13	ADCRST_I2	Current channel 2 simulates ADC reset control. 0: ADC is in normal working condition (default) 1: The ADC is in a reset state.
12	ADCRST_I1	Current channel 1 simulates ADC reset control. 0: ADC is in normal working condition (default) 1: The ADC is in a reset state.
11-10	VREF_BUFFER_CURS[1:0]	VREF Buffer current adjustment. 11: default power consumption (ADC clock EMUCLK, EMUCLKS=1) 10: Low power mode (ADC clock EMUCLK/4, EMUCLKS=1) 00: Ultra low power consumption patterns. =00（ADC clock 32K）
9-5	PGA_CURS[4:0]	PGA current adjustment. 00100: default power consumption (ADC clock EMUCLK,EMUCLKS=1) 01100: Low power mode (ADC clock EMUCLK/4, EMUCLKS=1) 11100: Ultra low power consumption patterns. =11100（ADC clock 32K）
4-0	ADC_CURS[4:0]	ADC current adjustment. 00100: default power consumption (ADC clock EMUCLK,EMUCLKS=1) 01100: Low power mode (ADC clock EMUCLK/4, EMUCLKS=1) 11100: Ultra low power consumption patterns. =11100（ADC clock 32K）

Bit Number	Bit Mnemonic	Description
23-0	EMUCFG2[23-0]	EMU configuration parameter register 2，Typical value is 0x0C84，low-power dissipation value is 0x098C

Table 9.47 EMU configuration parameter register 3:

33H	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
EMUCFG3	-	-	-	-	-	-	-	PD_BG
R/W	-	-	-	-	-	-	-	R/W
Reset Value（POR/WDT/LVR/PIN）	-	-	-	-	-	-	-	1 u 1 1
33H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUCFG3	EN_BG_CHOP	EN_BG_DEM	BG_CHOPCK_SEL.1	BG_CHOPCK_SEL.0	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/	1 u	1 u	1 u	0 u	1 u	0 u	0 u	0 u

PIN）	1 1	1 1	1 1	0 0	1 1	0 0	0 0	0 0

Bit Number	Bit Mnemonic	Description
8	PD_BG	VREF Enable =0,NORMAL MODE; =1,STOP MODE, default =0
7	EN_BG_CHOP	VREF CHOP Clock Enable Control, Default :1
5-4	BG_CHOPCK_SEL[1:0]	VREF CHOP clock select EMUCLKS=1X: 00: EMUCLK/64 01: EMUCLK /32 10: EMUCLK /16(default) 11: EMUCLK /8 EMUCLKS=01: 00: EMUCLK/4 01: EMUCLK/2 10: EMUCLK 11: EMUCLK

Bit Number	Bit Mnemonic	Description
15-0	EMUCFG3[15-0]	EMU configuration parameter register 3，Typical value is 0x0E8

Table 9.48 Channel 1 Active Power Gain Register

34H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
W1GAIN	W1GAIN.15	W1GAIN.14	W1GAIN.13	W1GAIN.12 ...2	W1GAIN.2	W1GAIN.1	W1GAIN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	W1GAIN[15:0]	Active power gain of channel 1,the binary complement means a signed value

The 15 bit is sign bit.

Table 9.49 Channel 1 Current Phase Compensation Register

35H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
P1CAL	P1CAL.15	P1CAL.14	P1CAL.13	P1CAL.12…3	P1CAL.2	P1CAL.1	P1CAL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	P1CAL[15:0]	Current phase compensation of channel 1, the binary complement means a signed value

phase compensation value: $\pm 2^{15} - 1$，The formula：

For 50Hz Signal，

$$PXCAL = round(\frac{1.16065 \cdot Err}{0.01636 + 0.58028 \cdot Err} \times 2^{15}) \quad (Err \geq 0)$$

0r

$$PXCAL = round(-\frac{1.14901 \cdot Err}{0.01636 - 0.57447 \cdot Err} \times 2^{15})$$ （Err < 0）

For 60Hz Signal，

$$PXCAL = round(\frac{1.16061 \cdot Err}{0.01963 + 0.58025 \cdot Err} \times 2^{15})$$ （Err ≥ 0）

or

$$PXCAL = round(\frac{1.14898 \cdot Err}{0.01963 - 0.57443 \cdot Err} \times 2^{15})$$ （Err < 0）

Table 9.50 Channel 2 Active Power Gain Register

36H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
W2GAIN	W2GAIN.15	W2GAIN.14	W2GAIN.13	W2GAIN.12…3	W2GAIN.2	W2GAIN.1	W2GAIN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	W2GAIN[15:0]	Channel 2 Active Power Gain Register，,the binary complement means a signed value

Table 9.51 Channel 2 Current Phase Compensation Register

37H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
P2CAL	P2CAL.15	P2CAL.14	P2CAL.13	P2CAL.12…3	P2CAL.2	P2CAL.1	P2CAL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	P2CAL[15:0]	Channel 2 Current Phase Compensation Register，,the binary complement means a signed value

Table 9.52 Current Gain Configuration of Channel 2

38H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
I2GAIN	I2GAIN.15	I2GAIN.14	I2GAIN.13	I2GAIN.12…3	I2GAIN.2	I2GAIN.1	I2GAIN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	I2GAIN[15:0]	Current Gain Configuration of Channel 2,the binary complement means a signed value

Comparing the current rms value of the two channels is needed at anti-tampering, so, the two current channel register should be equal when the same current input, and this can be completed by current gain of channel 2 configuration register I2GAIN. The current rms of channel 2 is the result of the calculated current rms of channel 2 multiplied by a coefficient (1 + I2GAIN/216).

Table 9.53 Active power offset of Channel 1

39H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
WATT1OS	W1OS.23	W1OS.22	W1OS.21	W1OS.20…3	W1OS.2	W1OS.1	W1OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	W1OS[23:0]	Active power offset of Channel 1，,the binary complement means a signed value

This register participate in the active power and energy calculation of channel 1

Table 9.54 Active power offset of Channel 2

3AH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
WATT2OS	W2OS.23	W2OS.22	W2OS.21	W2OS.20…3	W2OS.2	W2OS.1	W2OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	W2OS[23:0]	Active power offset of Channel 2,the binary complement means a signed value

This register participate in the active power and energy calculation of channel 2.

Table 9.55 Reactive power offset of Channel 1

3BH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VAR1OS	VAR1OS.23	VAR1OS.22	VAR1OS.21	VAR1OS.20	VAR1OS.2	VAR1OS.1	VAR1OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VAR1OS[23:0]	Reactive power offset of Channel 1，,the binary complement means a signed value

This register participate in the reactive power and energy calculation of channel 1.

Table 9.56 Reactive power offset of Channel 2

3CH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VAR2OS	VAR2OS.23	VAR2OS.22	VAR2OS.21	VAR2OS.20	VAR2OS.2	VAR2OS.1	VAR2OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VAR2OS[23:0]	Reactive power offset of Channel 2,the binary complement means a signed value

This register participate in the reactive power and energy calculation of channel 2.

Table 9.57 I1 RMS offset

3DH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
IRMS1OS	IRMS1OS.23	IRMS1OS.22	IRMS1OS.21	IRMS1OS.21 2	IRMS1OS.2	IRMS1OS.1	IRMS1OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	IRMS1OS[23:0]	Current RMS offset of Channel 1, the binary complement means a signed value

This register participate in the rms current channel 1 calculation. 1LSB corresponding to 32768 LSB (left shift 15 bits) of current rms.

Table 9.58 I2 RMS offset

3EH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
IRMS2OS	IRMS2OS.23	IRMS2OS.22	IRMS2OS.21	IRMS2OS.21 2	IRMS2OS.2	IRMS2OS.1	IRMS2OS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	IRMS2OS[23:0]	Current RMS offset of Channel 2, the binary complement means a signed value

This register participate in the rms current channel 1 calculation. 1LSB corresponding to 32768 LSB (left shift 15 bits) of current rms.

Table 9.59 Voltage RMS offset

3FH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VRMSOS	VRMSOS.23	VRMSOS.22	VRMSOS.21	VRMSOS.21 2	VRMSOS.2	VRMSOS.1	VRMSOS.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VRMSOS[23:0]	Voltage RMS offset,the binary complement means a signed value

This register participate in the rms voltage calculation. 1LSB corresponding to 64 LSB (left shift 6 bits) of voltage rms.

Table 9.60 ADC offset of current channel 1

40H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
ADCOSI1	OSI1.15	OSI1.14	OSI1.13	OSI1.12…3	OSI1.2	OSI1.1	OSI1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	OSI1[15:0]	ADC offset of current channel 1,the binary complement means a signed value

ADC offset metering position of current channel 2 is before high-pass filter in physics.

Table 9.61 ADC offset of current channel 2

41H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
ADCOSI2	OSI2.15	OSI2.14	OSI2.13	OSI2.12…3	OSI2.2	OSI2.1	OSI2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	OSI2[15:0]	ADC offset of current channel 2，the binary complement means a signed value

ADC offset metering position of current channel 2 is before high-pass filter in physics.

Table 9.62 ADC offset of voltage channel

42H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
ADCOSU	OSU.15	OSU.14	OSU.13	OSU.12…3	OSU.2	OSU.1	OSU.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	OSU[15:0]	ADC offset of voltage channel,the binary complement means a signed value

Table 9.63 Active power startup settings Registers

43H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
SPTSP	SPTSP.15	SPTSP.14	SPTSP.13	SPTSP.12…	SPTSP.2	SPTSP.1	SPTSP.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	SPTSP [15:0]	Threshold configuration for active power startup, unsigned value

If the average value of active power is greater than or equal to SPTSP, active power Registers began to accumulate, if the average active power is less than SPTS, active energy accumulation RegistersAERY, AERYL reset.

Table 9.64 Reactive power startup settings Registers

44H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
SPTSQ	SPTSQ.15	SPTSQ.14	SPTSQ.13	SPTSQ.12…	SPTSQ.2	SPTSQ.1	SPTSQ.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	SPTSQ [15:0]	Threshold configuration for reactive power startup, unsigned value

If the average value of reactive power is greater than or equal to SPTSQ, reactive power Registers began to accumulate, if less than the average reactive power SPTS, reactive power accumulator Registers reset.

Table 9.65 Voltage Constant

45H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
VCONST	VCONST.15	VCONST.14	VCONST.13	VCONST.12	VCONST.2	VCONST.1	VCONST.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	VCONST[23:0]	Voltage constant, unsigned value

If voltage sag, this register instead of the input voltage for active energy calculation. Corresponding the voltage channel.

Table 9.66 Voltage Sag Threshold

46H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
SAGTHR	SAGTHR.15	SAGTHR.14	SAGTHR.13	SAGTHR.12	SAGTHR.2	SAGTHR.1	SAGTHR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	SAGTHR[15:0]	Threshold configuration for voltage sag, unsigned value

Compare the detected voltage value with SAGTHR, if the voltage is less than SAGTHR or there is no zero-crossing of voltage in SAGCNT period of metering sampling, then the voltage sag occurs, set the voltage sag flag and into the state of voltage sag. The detected voltage value comes from the high 8 bits of the voltage channel ADC. In the state of voltage sag, if the voltage is

less than SAGTHR or there is no zero-crossing of voltage, the voltage sag flag is no longer set, otherwise,clear the voltage sag state.

Table 9.67 Voltage Sag Sampling Counting

47H	Bit15	Bit14	第13-9位	Bit8	Bit7	第6-1位	Bit0
SAGCNT	SAGCNT.15	SAGCNT.14	SAGCNT.13-8	SAGCNT. 8	SAGCNT.7	SAGCNT.6…1	SAGCNT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	1 u 1 1	1 u 1 1	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	SAGCNT[15:0]	Sampling count for voltage sag, unsigned value .Default :0x180

Table 9.68 Output Pulse Frequency

48H	Bit15	Bit14	Bit13	第12-8位	Bit7	第6-2位	Bit0	Bit0
ICONT	ICONT.15	ICONT.14	ICONT.13	ICONT.12-8	ICONT.7	ICONT.6…2	ICONT.1	ICONT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	1 u 1 1	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	ICONT[15:0]	Configuration for output pulse frequency, unsigned value, Default :0x80

If the ICONT set to 0, equal with 1 when the pulse compare

Table 9.69 Fast Active Pulse Counting

49H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
PCNT	PCNT.15	PCNT.14	PCNT.13	PCNT.12…3	PCNT.2	PCNT.1	PCNT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	PCNT[15:0]	Fast active pulse counting, the binary complement means a signed value

Table 9.70 Fast Reactive Pulse Counting

4AH	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
QCNT	QCNT.15	QCNT.14	QCNT.13	QCNT.12…3	QCNT.2	QCNT.1	QCNT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	QCNT[15:0]	Fast reactive pulse counting, the binary complement means a signed value

Table 9.71 Calculate cycle register

4BH	Bit15	Bit14	第13-10位	Bit9	Bit8	第7-1位	Bit0
SUMSAMPS	-	SAMP.14	SAMP.13-11	SAMP.10	SAMP.9-8	SAMP.7	SAMP.6-0

R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0 u 0 0	0 u 0 0	1 u 1 1	0 u 0 0	1 u 1 1	0 u 0 0

Bit Number	Bit Mnemonic	Description
14-0	SAMP[14:0]	Calculate cycle register, the binary complement means a unsigned value. Default 0x480 It is the max detection cycle of power, RMS, max ADC value. Reset value is 0x1FF.

The Registers set value computation formula is as follows:
If the expected calculation period is T(s), the setting value is T* update frequency, such as the update frequency is 19200Hz, and the calculation cycle 1s, the setting value is 19200(0X4B00).

Table 9.72 Active power const

4CH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
APCONST	APCST.23	APCST.22	APCST.21	APCST.20…	APCST.2	APCST.1	APCST.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	APCST[23:0]	Active power const, the binary complement means a unsigned value

Table 9.73 Reactive power const register

4DH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
RPCONST	RPCST.23	RPCST.22	RPCST.21	RPCST.20…	RPCST.2	RPCST.1	RPCST.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RPCST[23:0]	Reactive power const, the binary complement means a unsigned value

Table 9.74 Fast active pulse counter

4EH	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
PCNT_CONST	PCNT_ CONST.15	PCNT_ CONST.14	PCNT_ CONST.13	PCNT_ CONST.12…	PCNT_ CONST.2	PCNT_ CONST.1	PCNT_ CONST.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	PCNT_ CONST[15:0]	Fast active pulse counter, the binary complement means a signed value.

Table 9.75 Fast reactive pulse counter

4FH	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
QCNT_CONST	QCNT_ CONST.15	QCNT_ CONST.14	QCNT_ CONST.13	QCNT_ CONST.12…	QCNT_ CONST.2	QCNT_ CONST.1	QCNT_ CONST.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	QCNT_ CONST[15:0]	Fast reactive pulse counter, the binary complement means a signed value.

Table 9.76 DIMMER Determine threshold Settings.

50H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
DIMTHR	DIMTHR.23	DIMTHR.22	DIMTHR.21	DIMTHR.20 _3	DIMTHR.2	DIMTHR.1	DIMTHR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	DIMTHR [23:0]	DIMMER Determine the threshold setting, unsigned value, and the measurement module values the absolute value over DIMTHR in the set period. The number of times is counted, and when the number of statistics exceeds the DIMCNT set value, the DIMFLG is produced and the corresponding interrupt is generated.

Table 9.77 DIMMER Differential count threshold.

51H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIMCNT	DIMCNT.7	DIMCNT. 6	DIMCNT. 5	DIMCNT. 4	DIMCNT.3	DIMCNT.2	DIMCNT. 1	DIMCNT. 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （ POR/WDT/LVR/PIN）	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	1 u 1 1	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
7-0	DIMCNT [7:0]	DIMMER Differential count threshold.，nsigned value, Default value0x04

Table 9.78 EMU Waveform sampling Configuration Registerss:

52H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SAMPCON	-	-	SAMPF1	SAMPF0	SAMP2	SAMPS1	SAMPS0	SAMPON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （ POR/WDT/LVR/PIN）	-	-	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
5-4	SAMPF[1:0]	Waveform sampling frequency control. 00：CIC update frequency 01：CIC update frequency /4 10：CIC update frequency /8 11: CIC update frequency /16

3	SAMPS2	Waveform sampling data source control. 0：High-pass waveform data. 1：High-pass waveform data.
2-1	SAMPS[1-0]	Waveform sampling data source control. 00：Voltage channel 01：Current channel 1 10：Current channel 2 11：Voltage，Current 1，Current 2 Order record
0	SAMPON	Waveform sampling control enables the ability to trigger bits. 0：Waveform sampling is not started or completed. 1：Once the waveform sampling is triggered, the position will be reset automatically after sampling.

Table 9.84 High Pass coefficient B

5AH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
HPFEFFB	HPEF.23	HPEF.22	HPEF.21	HPEF.20-3	HPEF.2	HPEF.1	HPEF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	HPFE[23:0]	High Pass coefficient B (Default：0x800000)

Table 9.85 High Pass coefficient A Registers

5BH	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
HPFEFFA	HPEF.23	HPEF.22	HPEF.21	HPEF.20-3	HPEF.2	HPEF.1	HPEF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	HPFE[23:0]	High Pass coefficient A (Default：0x7FF547)

Table 9.86 Low pass coefficients B Registers

60H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
LPFEFFB	LPEF.23	LPEF.22	LPEF.21	LPEF.20-3	LPEF.2	LPEF.1	LPEF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	LPFE[23:0]	Low Pass coefficient B (Default：0x55D)

Table 9.87 Low Pass coefficient A Registers

61H	Bit23	Bit22	Bit21	Bit20~Bit3	Bit2	Bit1	Bit0
LPFEFFA	LPEF.23	LPEF.22	LPEF.21	LPEF.20-3	LPEF.2	LPEF.1	LPEF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	LPFE[23:0]	Low Pass coefficient A (Default：0x7FF546)

Table 9.81 Ultra-low power setting register (controls DIMMER and reactive power)

62H	Bit15	Bit14	Bit13	Bit12	Bit10	Bit10	Bit9	Bit8
ULPCTRL	-	-	-	-	-	-	-	-
R/W	-	-	-	-	-	-	-	-
Reset Value （POR/WDT/LVR/PIN）	-	-	-	-	-	-	-	-
62H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ULPCTRL	-	-	-	-	-	-	DIS_DIMMER_SEL	DIS_RPWR_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value （POR/WDT/LVR/PIN）	-	-	-	-	-	-	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
1	DIS_DIMMER_SEL	DIMMER's do not enable working options 0：enable 1：1: un-enabe
0	DIS_RPWR_SEL	Reactive power metering does not enable work selection 0：enable 1: un-enabe

Bit Number	Bit Mnemonic	Description
15-0	ULPCTRL[15-0]	Ultra-low power setting register，Default：0x00

Table 9.82 Channel 1 active power accumulative value high register

70H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
AERY1H	AERY1H.23	AERY1H.22	AERY1H.21	AERY1H.20 …3	AERY1H.2	AERY1H.1	AERY1H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description

23-0	AERY1H[23:0]	Channel 1 the cumulative value of active power is high, and the binary complement represents the signed number *Note: positive Numbers indicate positive work;A negative number means negative work*

Table 9.83 Channel 1 high register of accumulative value of reactive power

71H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
RERY1H	RERY1H.23	RERY1H.22	RERY1H.21	RERY1H.20 …3	RERY1H.2	RERY1H.1	RERY1H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY1H[23:0]	Channel 1 the accumulative value of reactive power is high, and the binary complement represents the signed number *Note: positive Numbers indicate positive work;* *A negative number means negative work*

Table 9.84 Channel 1 active power accumulator bit register

72H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
AERY1M	AERY1M.23	AERY1M.22	AERY1M.21	AERY1M.20 …3	AERY1M.2	AERY1M.1	AERY1M.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERY1M[23:0]	Channel 1 median of cumulative value of active power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.85 Channel 1 bit register of accumulative value of reactive power

73H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
RERY1M	RERY1M.23	RERY1M.22	RERY1M.21	RERY1M.20 …3	RERY1M.2	RERY1M.1	RERY1M.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY1M[23:0]	Channel 1 median value of accumulative value of reactive power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.86 Channel 1 active power accumulator low register

74H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
AERY1L	AERY1L.15	AERY1L.14	AERY1L.13	AERY1L.12 …3	AERY1L.2	AERY1L.1	AERY1L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	AERY1L[15:0]	Channel 1 low cumulative value of active power,The binary complement represents the signed number

Table 9.87 Channel 1 low register of accumulative value of reactive power

75H	Bit15	Bit14	Bit13	Bit12~3	Bit2	Bit1	Bit0
RERY1L	RERY1L.15	RERY1L.14	RERY1L.13	RERY1L.12 …3	RERY1L.2	RERY1L.1	RERY1L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	RERY1L[15:0]	Channel 1: low cumulative value of reactive power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.88 Channel 2 active power accumulative value high register

76H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
AERY2H	AERY2H.23	AERY2H.22	AERY2H.21	AERY2H.20 …3	AERY2H.2	AERY2H.1	AERY2H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERY2H[23:0]	Channel 2 active power accumulative value high register .The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.89 Channel 2 high register of accumulative value of reactive power

77H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
RERY2H	RERY2H.23	RERY2H.22	RERY2H.21	RERY2H.20 …3	RERY2H.2	RERY2H.1	RERY2H.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY2H[23:0]	Channel 2 the cumulative value of reactive power is high,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.90 Channel 2 active power accumulator bit register

78H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
AERY2M	AERY2M.23	AERY2M.22	AERY2M.21	AERY2M.20 …3	AERY2M.2	AERY2M.1	AERY2M.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	AERY2M[23:0]	Channel 2 median of cumulative value of active power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.91 Channel 2 middle register of accumulative value of reactive power

79H	Bit23	Bit22	Bit21	Bit20~3	Bit2	Bit1	Bit0
RERY2M	RERY2M.23	RERY2M.22	RERY2M.21	RERY2M.20…3	RERY2M.2	RERY2M.1	RERY2M.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
23-0	RERY2M[23:0]	Channel 2 median value of accumulative value of reactive power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.92 Channel 2 active power accumulator low register

7AH	Bit15	Bit14	Bit13	Bit 12-3	Bit2	Bit1	Bit0
AERY2L	AERY2L.15	AERY2L.14	AERY2L.13	AERY2L.12…3	AERY2L.2	AERY2L.1	AERY2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	AERY2L[15:0]	Channel 2 low cumulative value of active power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.93 Channel 2 low register of accumulative value of reactive power

7BH	Bit15	Bit14	Bit13	Bit 12-3	Bit2	Bit1	Bit0
RERY2L	RERY2L.15	RERY2L.14	RERY2L.13	RERY2L.12…3	RERY2L.2	RERY2L.1	RERY2L.0
R/W	R	R	R	R	R	R	R
Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	RERY2L[15:0]	Channel 2 low accumulative value of reactive power,The binary complement represents the signed number *Note: positive Numbers indicate positive work;*

Table 9.94 Output pulse frequency setting

7CH	Bit15	Bit14	Bit13	Bit12-8	Bit7	Bit 6-2	Bit0	Bit0
ICONT1	ICONT1.15	ICONT1.14	ICONT1.13	ICONT1.12…8	ICONT1.7	ICONT1.6…2	ICONT1.1	ICONT1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset Value (POR/WDT/LVR/PIN)	0 u 0 0	0 u 0 0	0 u 0 0	0 u 0 0	1 u 1 1	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
15-0	ICONT1[15:0]	Output pulse frequency setting, unsigned value, default value 0x80

If ICONT1 is set to 0, the impulse comparison is treated as 1.

Table 9.95 EMU metering configuration register 4

7DH	Bit15	Bit14	Bit13	Bit12	Bit10	Bit10	Bit9	Bit8
EMUCFG4	-	-	-	-	-	EN_ADDSEL	EN_WOFFSET	EN_ICONT1
R/W	-	-	-	-	-	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/PIN）	-	-	-	-	-	0 u 0 0	0 u 0 0	0 u 0 0
7DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUCFG4	-	-	-	-	-	EN_AVER_ADD	EN_DIV_DEFEND	EN_PWR_SEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value（POR/WDT/LVR/PIN）	-	-	-	-	-	0 u 0 0	0 u 0 0	0 u 0 0

Bit Number	Bit Mnemonic	Description
10	EN_ADDSEL	The power accumulation value interpolates the control bit 0: perform linear interpolation 1: No interpolation
9	EN_WOFFSET	ADC offset calibration register width selection 0: enables ADC offset calibration with a width of 2BYTE 1: ADC offset calibration with a width of 3BYTE
8	EN_ICONT1	Enablement of ICONT1 0: disable ICONT1 (two metering channels use ICONT register together) 1: enable ICONT1 (use ICONT the first way and ICONT1 the second way)
2	EN_AVER_ADD	Average accumulation mode enables selection 0: unenabled (instantaneous value accumulation mode) 1: enable (mean value accumulation mode)
1	EN_DIV_DEFEND	Single - phase three - wire mode (primary and secondary) separate anti - submarine enablement options 0: not enabled 1: can make
0	EN_PWR_SEL	Two ways of active power measurement enable choice 0: not enabled 1: can make
Bit Number	Bit Mnemonic	Description
15-0	EMUCFG4[15-0]	The EMU metering configuration register 4 is set to 0x00 by default

Note 1: if EN_PWR_SEL sets 1, it will be automatically identified according to the configuration of PWRSEL[1:0] in EMUCFG1 (and only if PWRSEL[1:0]=00 or 01).

For example, when PWRSEL[1:0]=00, then the accumulation source of the reactive accumulation channel automatically switches to the instantaneous active power of channel 2

When PWRSEL[1:0]=01, then the accumulation source of the reactive accumulation channel automatically switches to the instantaneous active power of channel 1

Note: the corresponding NoQLd bit, REVQ bit, RERY, RERYL, VARPA, QCNT, SPTSQ, QFIE bit, QFIF bit and QF output pulse in EMUSR are changed to active power attribute automatically.

Note 2: if EN_ICONT1 is set to 1, the first accumulation is controlled by ICONT, and the second accumulation is controlled by ICONT1. See figure 9.5.2 for details.

Note 3: if EN_WOFFSET sets 1, then the three ADC offset calibration registers at 40H ADCOSI1, 41H ADCOSI2 and 42H ADCOSU are changed from the original 2-byte width (signed number) to 3-byte width (signed number).
Note 4: after EN_AVER_ADD is set to 1, the properties in EMUCFG1 (bit5-4) are changed as follows:

5-4	PWRSEL[1:0]	Metering channel selection: 00: select the average power of channel 1 as the power metering and power accumulation source 01: select the average power of channel 2 as the power metering and power accumulation source 10: choose channel 1,2 average power algebra and as the electric energy measurement as the electric energy accumulation source 11: channel 1 and channel 2 are selected as the average power absolute value and as the electric energy measurement and accumulation source

Note 5: single-phase three-wire mode (Description with PWRSEL[1:0]= 11 and EN_AVER_ADD=0)
A. EN_DIV_DEFEND 0

(| channel 1 average active power absolute value |+| channel 2 average active power absolute value |)< SPTSP, at this point the accumulation register is cleared (the low 24 bits of the electrical energy accumulation register is cleared, the high 24 bits remain unchanged), that is, it does not accumulate.

(absolute value of average active power of channel | 1 is |+| channel 2 is |)>= SPTSP. At this point (absolute value of instantaneous active power of channel | channel 1 is |+ instantaneous active power of channel | channel 2 is |) is sent to the accumulation register for accumulation.

B. EN_DIV_DEFEND 1

A= (| channel 1 average active power absolute value |<SPTSP)?

0: instantaneous active power absolute value | of channel 1 of |

B= (| channel 2 average active power absolute value |<SPTSP)?

0: instantaneous active power absolute value | of channel 2 of |

A1= (| channel 1 average active power absolute value |<SPTSP)?

0: average active power absolute value | of channel 1 of |

B1= (| channel 2 average active power absolute value |<SPTSP)?

0: average active power absolute value | of channel 2 of |

If (A1+B1) is less than SPTSP, then the accumulation register is cleared (the low 24 bits of the electrical energy accumulation register are cleared, while the high 24 bits remain unchanged), that is, it is not accumulated.

If (A+B) >=SPTSP, then (A+B) is sent into the accumulation register to accumulate.

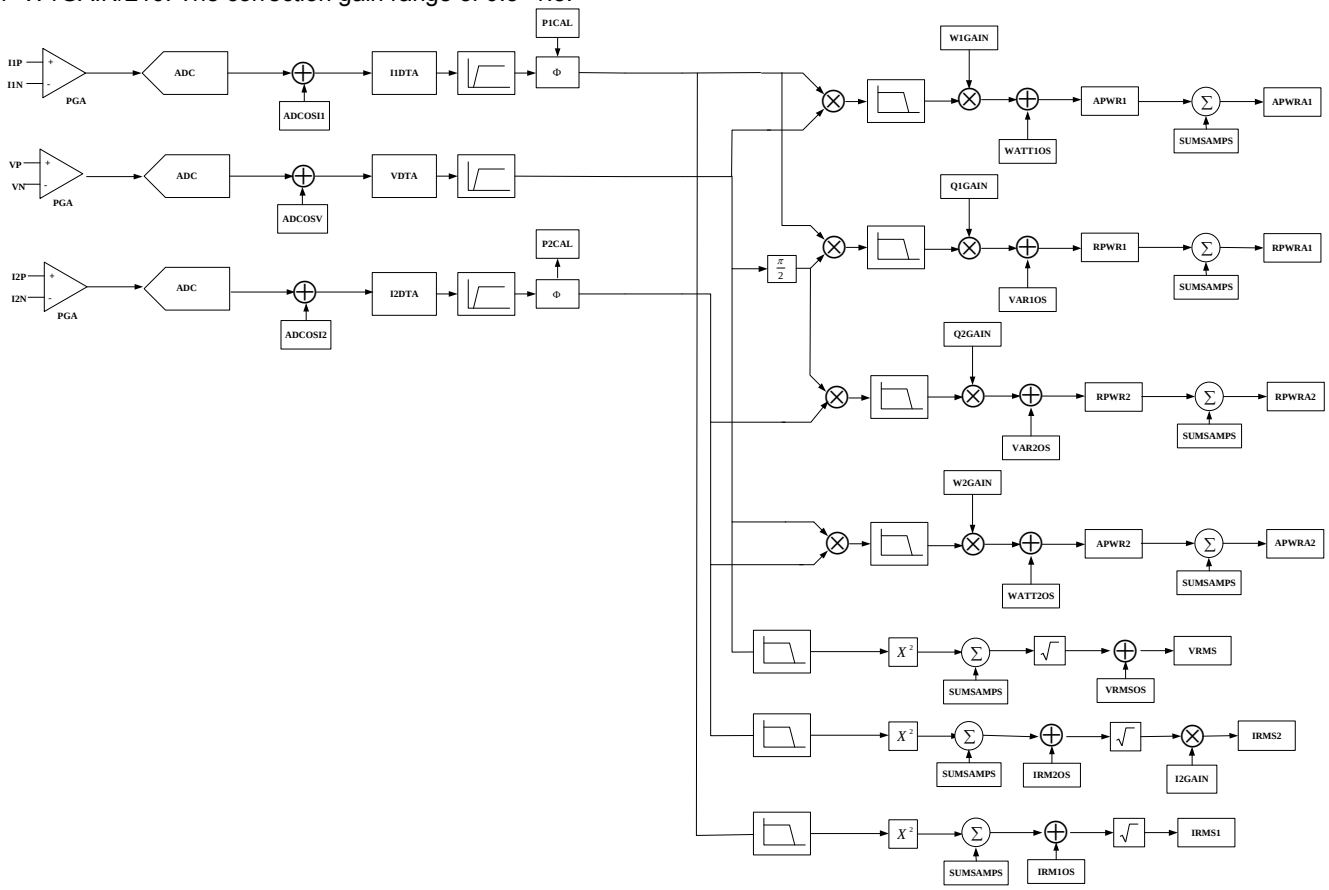
Note: if EN_DIV_DEFEND is enabled, such as a single-phase three-wire starting threshold such as (0.004*P), it is recommended to set the SPTSP to (0.0015*P).

9.5 Metering Function Description

EMU metering of active power, active energy, reactive power, reactive energy, voltage rms, current rms, corresponding correction function.

9.5.1 Active Power, Reactive Power

The voltage multiplied the current, and passed the low pass filter, then multiplied by the correction gain, the active power is achieved and stored to the register APWR1/APWR2. The high bit of W1GAIN and W2GAIN is sign bit, and correction gain is 1+W1GAIN/216. The correction gain range of 0.5~1.5.

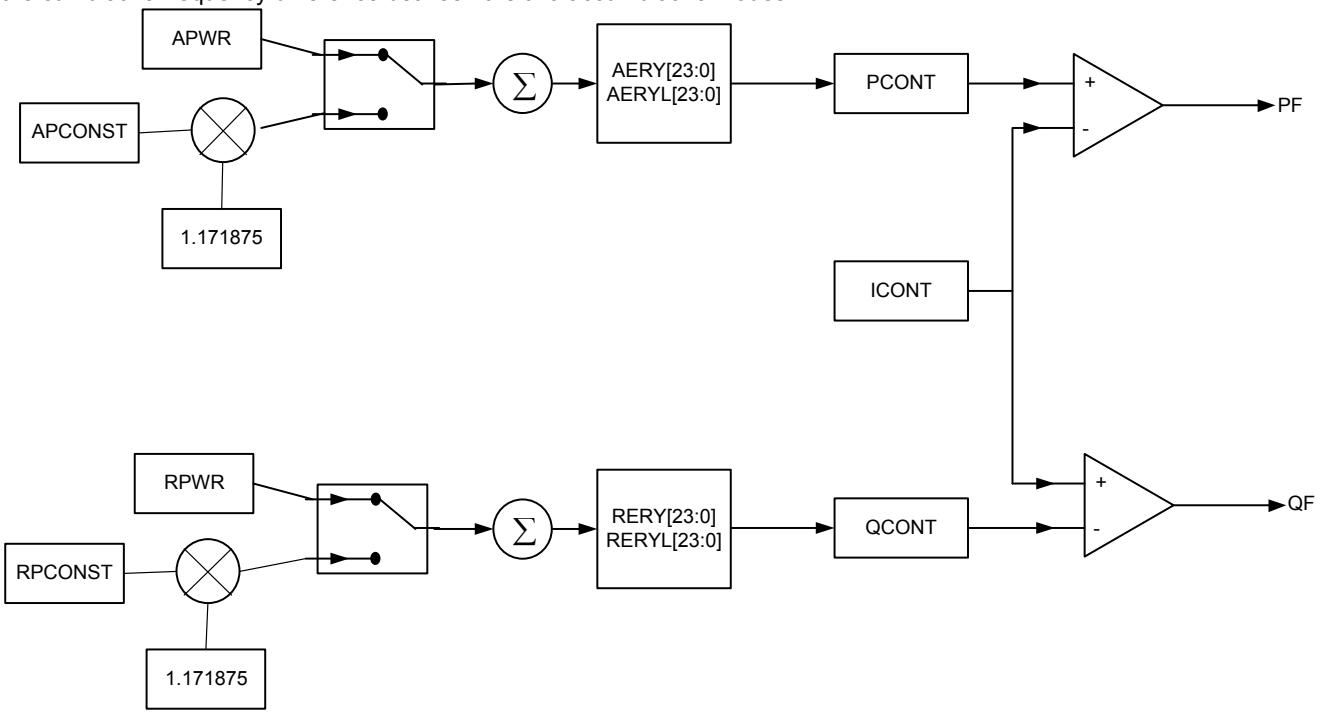


The active (reactive) power average value is calculated by a cycle time which set by SUMSAMPS register. The same to voltage RMS and current RMS value.

9.5.2 Energy and Pulse Output

The internal active energy register of 48bits, the highest bit is sign bit, to accumulate active power.The active energy value register (AERY) is high 24 bits of the internal active energy register, and the value back to 0 after overflowed.
The internal reactive energy register of 41bits, the highest bit is sign bit, to accumulate reactive power.The reactive energy value register (RERY) is high 24 bits of the internal reactive energy register, and the value back to 0 after overflowed.
By the conversion of the active and reactive energy, the corresponding proportion pulse output from PF and QF pin.
The energy can select 3 cumulative mode of forward, absolute value and algebraic sum metering through the QMOD and PMOD of EMCON.

There are two source of energy accumulation, one is active power value of present metering channel, the other is the const value which store in APCONST/RPCONST. APCONST/RPCONST accumulates a fixed gain of 1.171875 to compensate for the cumulative frequency difference between the two accumulative modes.



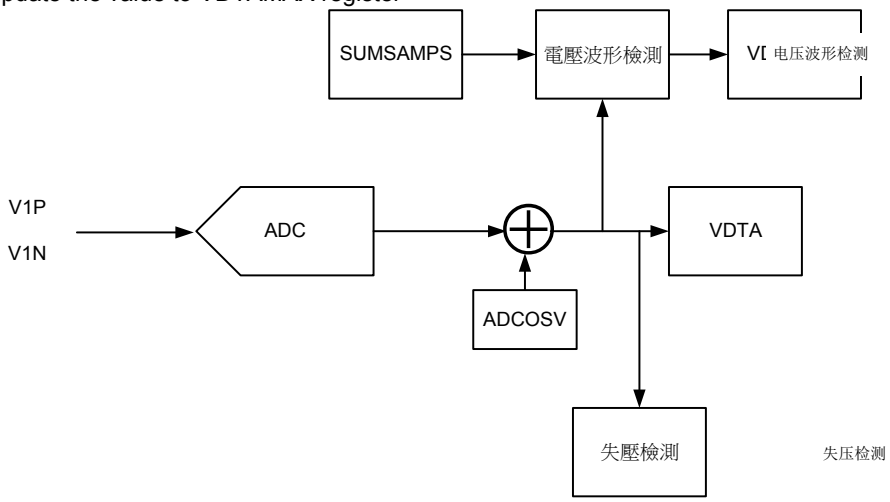
The active energy accumulating, the fast active pulse register PCNT increase 1LSB when the 23 bit (least significant bit to 0) of the internal active energy register increase 1, and if the absolute value of the register is greater than or euqal to the the value of ouput pulse frequence configuration register, outputing an active pulse of PF, setting PFIF(EMUIF.3) to 1, and the corresponding energy pulse accumulated register plus 1, the absolute active energy pulse accumulated register plus 1, clear REVP flag.
The active energy accumulating, the fast active pulse register PCNT decrease 1LSB when the 23 bit (least significant bit to 0) of the internal active energy register decrease 1, and if the absolute value of the register is greater than or euqal to the the value of ouput pulse frequence configuration register, outputing an active pulse of PF, setting PFIF(EMUIF.3) to 1, and the corresponding energy pulse accumulated register plus 1, the absolute active energy pulse accumulated register plus 1, set REVP flag to 1.
The reactive energy accumulating, the fast reactive pulse register QCNT increase 1LSB when the 23 bit (least significant bit to 0) of the internal reactive energy register increase 1, and if the absolute value of the register is greater than or euqal to the the value of ouput pulse frequence configuration register, outputing an reactive pulse of QF, setting QFIF(EMUIF.4) to 1, and the corresponding energy pulse accumulated register plus 1. the absolute reactive energy pulse accumulated register plus 1, clear REVQ flag.
The reactive energy accumulating, the fast reactive pulse register QCNT decrease 1LSB when the 23 bit (least significant bit to 0) of the internal reactive energy register decrease 1, and if the absolute value of the register is greater than or euqal to the the value of ouput pulse frequence configuration register, outputing an reactive pulse of QF, setting QFIF(EMUIF.4) to 1, and the corresponding energy pulse accumulated register plus 1. the absolute reactive energy pulse accumulated register plus 1, set REVQ flag to 1.
The reverse of active and reactive energy can be indicated by the REVP and RECQ of the status/control register EMUSR. When active pulse output, update REVP, and update REVQ when reactive pulse output.
The NoQld and NoPld of EMUSR could display the state of energy startup in real time, and the threshold selection will be easier.

9.5.3 Off Neutral Wire Mode

If the off neutral wire mode is enabled. Use the value in VCONST register (instead of ADC sampling value of voltage channel) to calculate active/reactive power value.

9.5.4 MAX ADC Sampling Value Record of Voltage Channel

In a sampling period (set by SAMSAMPS register), record the max ADC sampling absolute value of voltage channel and update the value to VDTAMAX register



9.5.5 single Phase 3 Wire Metering Mode

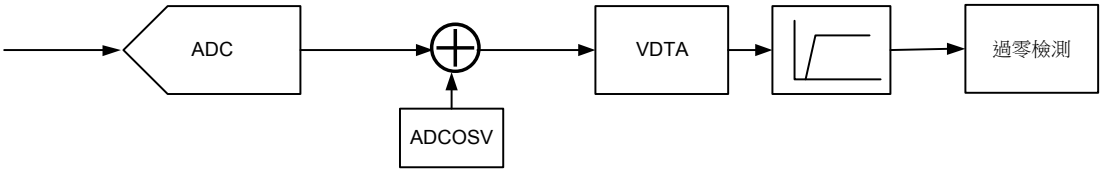
In this metering mode, APWR (RPWR) is sum of channel 1 and channel 2's active (reactive) power value. And the add mode can be absolute value added or not. The revise method can be found in the application manual.

9.5.6 Voltage Sag Detection

When ADC Sampling Value of Voltage Channel do not catch zero crossing point or the absolute max value less than SAGTHR value, in the period which set by SAGCNT, voltage sag happened, set SAGF and SAGIF to 1. Or clear SAGF and set SAGIF to 0.

9.5.7 Zero Crossing Detection

Zero crossing point detect by ADC Sampling Value of Voltage Channel, filtering the direct current component is necessary.



9.5.8 DIMMER Function

Dimmer SUMSAMPS detection Function is to set the cycle of sampling values of voltage channel according to the specific algorithm, get the second order differential voltage sampling and according to the set cycle second-order difference surpassed the threshold (DIMTHR) the number of times to determine whether there is a power theft.

The algorithm is as follows::

retain the latest three voltage channel ADC sampling values,VDATA(n-2), VDATA(n-1), VDATA(n)

calculate Y1= VDATA(n)-VDATA(n-1),Y2= VDATA(n-1)- VDATA(n-2)

calculate Y0=|Y1-Y2|

if Y0>DIMTHR, dimcounter++

if found in the sampling period.dimcounter>DIMCNT，则DIMFLG=1， interrupt

9.5.9 Waveform sampling record function

By setting the EMUCFG2 wavestart position, can trigger a waveform sampling, a waveform sampling will record the ADC output, can be achieved by SAMPCONRegistersSAMPF choose waveform sampling frequency (1-0), also can choose by SAMPS2 control bit ADC output and qualcomm qualcomm before data after the data, also can through the SAMPS (1-0) select records of voltage or current waveform is 1 or 2 or 3 channel current record at the same time, record the maximum length of 1536 byte, the starting address of 1 f00h, when the waveform sampling is completed, will generate the corresponding interrupt, and SAMPON reset, the waveform sampling period, no access to the RAM area by the user.

9.5.10 High /low pass coefficient configuration gear.

High Pass coefficient：

Working mode	B	A
ADCCKSEL[1:0]=00 (the effective value converges for a long time)	800000H	7FF547H
ADCCKSEL[1:0]=00 (the effective value converges for a short time)	800000H	7FBE77H
ADCCKSEL[1:0]=10	7FC4EAH	7F89D4H

Low Pass coefficient：

Working mode	B	A
ADCCKSEL[1:0]=00 (the effective value converges for a long time)	55DH	7FF546H
ADCCKSEL[1:0]=00 (the effective value converges for a short time)	2DE0H	7FA440H
3 ADCCKSEL[1:0]=10	216CH	7FBD28H

9.6 EMU Interrupt System

EMU supply 7 interrupts： DIM，QF，PF，SAG，SAMP，ZX，DSP。

SAG: When the line voltage sag is detected, set SAGIF flag of EMUIF register to 1

ZX: When the line voltage zero-crossing is detected, set ZXIF flag of EMUIF register to 1

DSP: When the DSP performs over, set DSPIF flag of EMUIF register to 1

The 7 interrupt request flags of EMU are all generated aftet a metering cycle, and share a common EMU interrupt. If EMUIE and the corresponding bit of EMUIF are 1, set the energy metering interrupt request flag EMUF(EXF0.6), if the energy metering interrupt enable flag EEMU(IEN1.0) is 1, EMU interrupt. Write 0 to the corresponding bit of EMUIF when clearing the interrupt request flag, if the result of EMUIF AND EMUIE is 0, then clear EMUF.

Table 9.100 EMU interrupt enable register

96H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUIE		DIMIE	DSPIE	QFIE	PFIE	SAMPIE	SAGIE	ZXIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6	DIMIE	DIMMER Detect interrupt Enable bit 0：Ban Dimmer Detect interrupt 1：allow Dimmer Detect interrupt
5	DSPIE	The interrupt enable of the end of DSP performing 0：Disable DSP end interrupt 1：Enable DSP end interrupt
4	QFIE	The interrupt enable of reactive pulse output 0：Disable reactive pulse output interrupt 1：Enable reactive pulse output interrupt
3	PFIE	The interrupt enable of active pulse output 0：Disable active pulse output interrupt 1：Enable active pulse output interrupt
2	SAMPIE	Waveform sampling Detect interrupt Enable bit 0：The cumulative cycle interruption is prohibited. 1：Allows cumulative cycles to be interrupted.
1	SAGIE	The interrupt enable of voltage sag 0：Disable voltage sag interrupt 1：Enable voltage sag interrupt
0	ZXIE	The interrupt enable of zero-crossing 0：Disable zero-crossing interrupt 1：Enable zero-crossing interrupt

Table 9.101 EMU interrupt request register

97H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EMUIF		DIMIF	DSPIF	QFIF	PFIF	SAMIF	SAGIF	ZXIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description

6	DIMIF	DIMMER To interrupt the request sign. 0：No interrupt flag 1：Interrupt flag
5	DSPIF	DSP Execution ends the interrupt request flag. 0：No interrupt flag 1：Interrupt flag
4	QFIF	The interrupt request flag of reactive pulse output 0：No interrupt flag 1：Interrupt flag
3	PFIF	The interrupt request flag of active pulse output 0：No interrupt flag 1：Interrupt flag
2	SAMPIF	Waveform sampling interrupt request flag. 0：No waveform sampling is suspended. 1：Interrupt flag
1	SAGIF	The interrupt request flag of voltage sag 0：No interrupt flag 1：Interrupt flag
0	ZXIF	The interrupt request flag of zero-crossing 0：No interrupt flag 1：Interrupt flag

10. Instruction Set

ARITHMETIC OPERATIONS				
Opcode	Opcode	Opcode	Opcode	Opcode
ADD A, Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A, direct	Add direct byte to accumulator	0x25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data	Add immediate data to accumulator	0x24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data	Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	2	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	1	3
INC DPTR	Increment data pointer	0xA3	1	4
MUL AB 8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB 8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A	Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS				
Opcode	Opcode	Opcode	Opcode	Opcode
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	Opcode	Opcode	Opcode	Opcode
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES				
Opcode	Opcode	Opcode	Opcode	Opcode
ACALL addr11	Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16	Long subroutine call	0x12	3	7
RET	Return from subroutine	0x22	1	8
RETI	Return from interrupt	0x32	1	8
AJMP addr11	Absolute jump	0x01-0xE1	2	4
LJMP addr16	Long jump	0x02	3	5
SJMP rel	Short jump (relative address)	0x80	2	4
JMP @A+DPTR	Jump indirect relative to the DPTR	0x73	1	6
JZ rel (not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel (not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel (not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel (not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit,rel (not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit,rel (not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel (not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A,direct,rel (not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A,#data,rel (not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn,#data,rel (not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri,#data,rel (not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn,rel (not aken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct,rel (not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP	No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	Opcode	Opcode	Opcode	Opcode
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

11. Electrical Characteristics

Absolute Maximum Ratings

DC Supply Voltage . . . . . -0.3V to +6.5V

Input / Output Voltage. . . . . DGND-0.3V to VOUT+0.3V

Analog input voltage . . . . . AGND-0.3V to AVDD+0.3V

Operating Ambient Temperature. . . . . -40°C to +85°C

Store Temperature. . . . . -55°C to +125°C

* Comments

Stresses exceed those listed under “Absolute Maximum Ratings” may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (VDD = 2.3- 5.5V, DGND = AGND = 0V, VBAT = 2.3 - 3.6V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	VDD	2.3	5	5.5	V	32.768kHz ≤ fSYS ≤ 9.8304MHz
Battery Voltage	VBAT	2.3	3.6	5.5	V	32.768kHz ≤ fSYS ≤ 9.8304MHz
法拉电容电压	VFCAP	2.3	5	5.5	V	32.768kHz ≤ fSYS ≤ 9.8304MHz
Operating Current	IOP1	-	-	800	μA	fsys = Fsys/12, PLL on All output pins unload(including all digital input pins un-floating), CPU on (execute NOP instruction), LCD on,WDT on , LVR on, LPD on, EMU on, RTC on, disable other fuctions, VDD =3.3V, VBAT=3.3V.
Stand by Current (IDLE)	ISB1	-	9	15	μA	fsys = 32.768kHz, PLL off All output pins unload(including all digital input pins un-floating)LCD off, WDT off, LVR on, RTC on, LPD on, disable other fuctions；VDD = 5V，VBAT = 3.3V
Stand by Current (Power-Down)	ISB2	-	-	3.5	μA	fOSC = 32.768kHz,PLL off All output pins unload(including all digital input pins un-floating), LCD off, RTC off, WDT off, LVR on, disable other fuctions；VDD = 5V，VBAT = 3.3V
WDT Current	IWDT	-	-	1	μA	All output pins unload；watchdog on VDD = 5 V
LCD Current 1	ILCD1	-	3	5	μA	Traditional LCD mode,VLCD = 3.0V 900k LCD bias, contrast [2:0] = 000 （Not include LCD panel）
LCD Current 2	ILCD2	-	7	9	μA	LCD Fast charge mode，VDD = 3.0V 900k LCD bias，1/16 LCD com period，contrast[2:0] = 111（Not include LCD panel）
Input Low Voltage 1	VIL1	GND	-	0.3×VDD	V	I/O port
Input high Voltage 1	VIH1	0.7×VDD	-	VDD	V	I/O port
Input Low Voltage 2	VIL2	GND	-	0.2×VDD	V	$\overline{RST}$，T0，T1，T2，T2EX，INT40~INT47, RXD0，RXD1，RXD2，RXD3，7816IO0，7816IO1 SCK，MISO，MOSI，$\overline{SS}$，（Schmitt trigger）
Input high Voltage 2	VIH2	0.8×VDD	-	VDD	V	$\overline{RST}$，T0，T1，T2，T2EX，INT40~INT47, RXD0，RXD1，RXD2，RXD3，7816IO0，7816IO1 SCK，MISO，MOSI，$\overline{SS}$，（Schmitt trigger）
Input Leakage Current	IIL	-1	-	1	μA	No pull-high, VIN= VDD or DGND
Pull-high Resistor	RPH1	-	30	-	kΩ	VDD = 5V，VIN = DGND
	RPH2	-	1	-	MΩ	VDD = 5V，VIN = DGND(P0，P2 Special mode)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Output high Voltage 1	VOH1	VDD - 0.7	-	-	V	I/O port，IOH = -10mA，VDD = 5.0V
	VOH2	VDD - 0.7			V	I/O port，IOH = -0.14mA，VDD = 5.0V （P2，P0 lower mode）
Output low Voltage 1	VOL1	-	-	GND + 0.6	V	I/O port，IOL = 15mA，VDD = 5.0V
	VOL2			GND + 1.5	V	IOL = 0.8mA，VDD = 5.0V(P1 Driver lower mode)

3.3V A/D Converter Electrical Characteristics

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Supply voltage	VAD	2.8	5	5.5	V	
Resolution	NR	-	10	-	bit	GND ≤ VAIN ≤ 1.4V
A/D Input Voltage	VAIN	GND	-	1.4	V	
A/D Input Resistor*	RAIN	2	-	-	MΩ	VIN = 1V
A/D conversion current	IAD	-	1	3	mA	ADC模块工作，VOUT = 5V
A/D Input current	IADIN	-	-	10	μA	VOUT = 5.0V
Analog voltage source is recommended impedance	ZAIN	-	-	10	kΩ	
Total Absolute error	EAD	-	-	±4	LSB	VOUT =5.0V
Total Conversion time**	TCON	28	-	-	ms	10bit，VOUT = 5.0V

*: "Typical" data is measured at 5V，25°C ，unless otherwise specified。

Analog Front-End Electrical Characteristics of Energy Metering
(VDD = 3.0 – 5.5V, DGND = AGND = 0V, TA = -40°C to +85°C, fSYS =9.8304MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Supply voltage	VAV	3.0	5	5.5	V	
Input signal level	I1P/I1N I2P/I2N VP/VN	-		±200	mV peak	PGA = 2
input impedance	RAV	80	250	-	kΩ	PGA = 2（*1）
PGA gain error	EPGA	-	-	±3	%	25°C，GAIN = 2、4、8、16
PGA Input offset	VOFF	-5	-	5	mV	GAIN = 2
		-0.5	-	0.5	mV	GAIN = 16

Electrical energy measurement simulation of the front end VREF electrical characteristics.
(VDD = 3.0 – 5.5V, DGND = AGND = 0V, TA = -40°C to +85°C, fSYS =9.8304MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Reference voltage output voltage.	VREF	1.19	1.201	1.21	V	25°C
The reference voltage temperature coefficient.	TCREF	-	±25	±44	PPM/°C	（*2）
Output impedance	RO	-	2		kΩ	

Base voltage annual rate.	Age		±25		PPM /year	（*2）
VREF Set up the time	Ton			100	mS	

Note: "*2" indicates that the index is designed to ensure that the mass production is not tested.

Accuracy of Energy Metering

(VDD = 3.0V – 5.5V, DGND = AGND = 0V, TA = -40°C to +85°C, fSYS = 9.8304MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Active energy metering error	EACT	-	0.1	-	%	Dynamic range of 3000:1 at 25℃
Reactive energy metering error	EREA	-	0.1	-	%	Dynamic range of 1500:1 at 25℃
Voltage RMS metering error	EVRMS	-	0.5	-	%	Dynamic range of 1500:1 at 25℃
Current RMS metering error	EIRMS	-	0.5	-	%	Dynamic range of 1500:1 at 25℃

Power supply switch electrical characteristics

(VDD = 2.3V – 5.5V, DGND = 0V, VBAT = 2.3V – 3.8V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Switch operating voltage range	VOUT	2.2	-	5.5	V	
VIN switching threshold voltage	VVIN	1.1	1.2	1.3	V	
VDD/VBAT switching threshold voltage	VSW1	2.9	3.0	3.1	V	
VDD/FCAP/VBAT Switch back to the poor	VSWS		50	75	mV	
Switch leakage current	ISW	-	10	-	nA	VBAT = 0，VOUT = 5V
VDD to VBAT switch delay (VDD detection control)	TVDDD	-	20	-	μs	VDD < 3V
VBAT to VDD switching delay	TBATD	-	8	-	μs	VDD > 3V
VDD to VOUT resistance	RVDO	-	-	10	Ω	VDD = 3.0V
VFCAP to VOUT resistance	RVDO	-	-	10	Ω	VFCAP= 3.0V
VBAT to VOUT resistance	RBATO	-	-	10	Ω	VBAT = 3.0V
VBAT leakage current	IVBAT	-	-	1	μA	VDD = 5.5V，VOUT = VDD, VFCAP = 5.5V

AC Electrical Characteristics

(VOUT = 2.3V – 5.5V, DGND = 0V, TA = 25°C, fOSC = 32.768kHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Oscillator Start time	TOSC	-	1	2	s	oscillator = 32768Hz
PLL Start time	Tpll	-	2	-	ms	Does not include oscillator start-up
PLL jitter(Period)	-	-	1	-	ns	oscillator = 32768Hz
RST pulse width	tRESET	10	-	-	μs	Active-low

RESET pin Pull-high Resistor	| Δ F|/F	-	±0.5	±1	%	8MRC oscillator： |F –8MHz|/8MHz （VDD = 2.2~5.0V，TA = -40°C至+85°C）

Low Voltage Reset Electrical Characteristics
(VOUT = 2.3V – 5.5V, DGND = 0V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
LVR voltage	VLVR	2.2	2.3	2.4	V	LVR enabled，VOUT = 2.3V – 5.5V
LVRReturn difference voltage	VHSY	-		100	mV	LVR enabled，Ta=25°C
LVR low voltage reset width	TLVR	-	30	-	μs	

32.768Hz Crystal Characteristics
(VOUT = 2.3V – 5.5V, DGND = 0V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Frequency	F32K	-	32768	-	Hz	
Load capacitance	CL	-	12.5	-	pF	
Driving power	P			1	uW	
Crystal series impedance	Rload			75	KΩ	25℃ ，VDD =3V

Temperature sensor
(VDD = 2.3V – 5.5V, GND = 0V, VBAT = 2.2V - 3.6V, TA = -40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Temperature sensor error.	TRSENSOR	-1	-	1	℃	-25°C ≤ TA ≤ 65°C，VDD = 3.0V – 5.5V VBAT = 3.0V – 3.6V，
Temperature sensor conversion time.	TCONR	-	-	400	mS	TA = 25°C，VDD = 5.5V，

Touch key electrical characteristics1.
(VDD = 2.3V -5.5V， GND = 0V， TA = +25°C，unless otherwise specified。)

Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Operating Voltage	VDD	2.4V	-	5.5	V	
Output Voltage1	VDDR1	2.9	3.0	3.1	V	IVDDR1=0~10mA , VDD=3.0~5.5V
Output Voltage 2	VDDR2	2.4	2.5	2.6	V	IVDDR2=0~10mA，VDD=3.0~5.5V
Output Voltage 3	VDDR3	1.9	2.0	2.1	V	IVDDR3=0~10mA，VDD=2.5~5.5V
Output Voltage 4	VDDR4	1.4	1.5	1.6	V	IVDDR4=0~10mA，VDD=2.4~5.5V
Output reference voltage 1	Vref1	0.9	1.0	1.1	V	VDD=2.4~5.5V
Output reference voltage 2	Vref2	1.1	1.2	1.3	V	VDD=2.4~5.5V
Output reference voltage 3	Vref3	1.5	1.6	1.7	V	VDD=2.4~5.5V
Output reference voltage 4	Vref4	1.9	2.0	2.1	V	VDD=2.4~5.5V

12. Product naming rules

G 80 F975A

75A: Product serial number
9： Electricity meter measurement class MCU
F： Flash series
80： 8051 core
G： GREEN CHIPS

NL84S-2

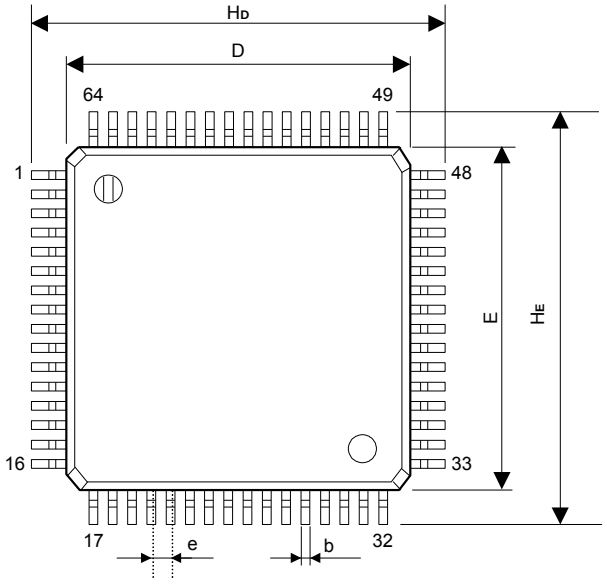
Lot number
The number of characters of lot number varies between 0 to 9 and the letters vary from A to Z.

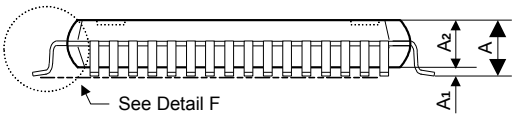
1929-Y

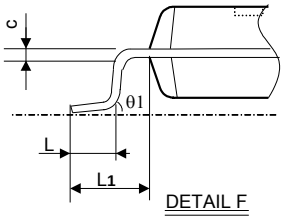
19 :Year
29 :Week
Y:Production code

13. Package Information

LQFP 64L Outline Dimensions
Unit：Inch /mm







Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	---	0.063	---	1.600
A1	0.002	0.006	0.050	0.150
A2	0.053	0.057	1.350	1.450
D	0.272	0.280	6.900	7.100
E	0.272	0.280	6.900	7.100
HD	0.346	0.362	8.800	9.200
HE	0.346	0.362	8.800	9.200
b	0.007	0.009	0.170	0.240
e	0.016BSC		0.400BSC	
c	0.004	0.008	0.090	0.200
L	0.018	0.030	0.450	0.750
L1	0.033	0.045	0.850	1.150
	0°	10°	0°	10°

14. Datasheet Document History

Version	Record	Date
V1.00	Original Version	2019.12

15. Business contact

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16. Disclaimer

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